Edge-TCT measurements on irradiated HV CMOS sensors
CERN Summer Student Report

Constantin Weisser
CERN Summer Student

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Abstract

Passive $100 \times 100 \mu m$ test diodes in an unirradiated and an irradiated HV2FEI4v3 HV-CMOS silicon sensor were analysed using the edge TCT technique. To integrate the sensor into the setup a PCB was designed to extract the signals, a cooling mechanism was constructed and the system housed in a shielding box.

The observed signal had fast and slow contributions, that were interpreted as drift and diffusion. The former peaked in a region, that was interpreted as the depletion region, while the latter peaked further in the bulk material. Raising the bias voltage increased the depth of the former region, while pushing the latter region further into the bulk.

The irradiated sample lost signal strength mainly in its slow part compared to the unirradiated sample, while its quick signal remained largely unaffected. As only the signal interpreted as drift is fast enough to be useful in LHC operation the investigated sensors could be considered radiation hard for this purpose. This gives further promise to the HV CMOS technology for high energy physics applications.
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1 The need for cheap, radiation hard detectors

The Large Hadron Collider (LHC) at the research organisation CERN is the most energetic particle collider in the world. However, in order to further probe the laws of particle physics it is due to be upgraded in 2022 to reach even higher luminosities and an order of magnitude larger statistics.

The result of higher numbers of particles passing through the four main detector experiments will require increased granularity in the sensors that detect incoming particles. Because high granularity sensors are expensive and large areas need to be covered, research has been done into comparably cheap industrial processes of producing sensors.

Radiation knocks silicon atoms out of their lattice in the sensor and thereby induces defects. Free electrons and holes can be trapped temporarily, which reduces the signal. Because with the new upgrade 10 times more particles will pass through the sensors (more fluence) the chips should degrade as little as possible when irradiated. They have to be radiation hard. This project was about investigating the radiation hardness of HV CMOS detectors with a look at the time-resolved diode current revealing the charge collection process.

2 HV2FEI4v3

One candidate of a competitively priced, industrial technique for producing silicon sensors is the High Voltage Complementary Metal-Oxide-Semiconductor (HV CMOS) process (see figure 1). In industry this method is used for ASIC production for the automotive industry.

The chip being investigated was developed by Ivan Perić at the University of Heidelberg in Germany. It consists of pixel matrices, amplifiers and other components like a single square passive test diode of 100 µm length for testing purposes (see figure 2). This diode should be representative of a normal pixel and was used for this investigation. One complication was that there was no “shielding” provided by neighbouring diodes under real conditions. When applying the bias voltage (= “high voltage”) a region around the chip was slowly depleted, not only the region directly beneath the diode,
Figure 2: Top down view onto the 2.725 mm long and 2.298 mm wide HV2FEI4v3 chip. The red arrow points at the passive test diode, that was the focus of this line of research.

which would happen if it was immersed in a pixel matrix. For that reason, shielding diodes might be added to the next version of the chip. Two samples were looked at. The first was not irradiated, while the other had experienced a fluence of $1 \times 10^{15} \text{Neq cm}^{-2}$ (1 MeV Neutron equivalents per square centimetre) in the TRIGA research centre of the JSI Ljubljana.

3 Edge - TCT

In order to simulate particles created by LHC collisions the edge transient current technique (eTCT = Edge TCT) was utilised. Photon pulses from an infrared laser shot into the side of the sensor were focussed in the chip as shown in figure 3. These photons created electron-hole pairs. Because of the electric field in the detector the particles moved in opposite directions and their motion induced an electric current, which was detected (see figure 4). The signal was then analysed using an amplifier, an oscilloscope and an attached computer.

3.1 Edge - TCT Setup

In order to perform this experiment the following components were needed (see figures 5 and 6).

- ETS Lindgren Faraday Cage
3.1 Edge - TCT Setup

Figure 3: The edge - TCT concept with measurement in the high voltage branch. Source: Nicola Pacifico

Figure 4: Incoming radiation creates electron - hole pairs whose motion is detected. Not to scale

- PicoQuant LDH-P-C 1060 laser
- PicoQuant PDL 800-B Diode laser driver
- Agilent B1104A Pattern Generator
- Agilent DSO9254A Oscilloscope
- Cividec C2HV0131 amplifier
- Agilent B1104A amplifier power supply
- Keithley 2410 to provide bias voltages
- NI CB-68LP Connector Block for PC communication for the Peltier
- Peltier power supply
- ESP301 Motion controller and stages
- Handmade Relay box for Peltier
- Detector box with sensor inside
3.1 Edge - TCT Setup

Figure 5: The whole eTCT setup

Figure 6: The inside of the eTCT Faraday cage
3.2 Types of scans

With this setup the position of the focus of the laser could be varied in all three spacial dimensions and different bias voltages could be applied. The x direction was defined to be along the edge of the sensor, the y direction was the focus dimension and z was the in along the depth of the sensor. ZY scans were used for finding the focus. XZ scans were for finding out the position and dimensions of the sensor and ZV scans provided information about the signals’ dependence on bias voltage.

4 Detector box

In order to characterise the HV CMOS chip it had to be integrated into the existing edge - TCT setup. This was done by building a detector box to house the chip (see figure 7). To be able to cool the chip down a Peltier element was placed under the chip. Peltier elements act as a heat pump cooling the top side and heating up the bottom side when a voltage is applied (or the other way around). To extract the excess heat on the hot side a cooling bock was placed under the Peltier element. Plastic plates provided insulation and a metal box acted as a Faraday cage and protected the sensor from mechanical dangers. The dimensions of the components can be seen in figures 8 and 9.

However, the main part of the detector box was a Printed Circuit Board (PCB) that was designed to provide the chip with a bias voltage and extract the signal of the detector. The unirradiated sensor was wirebonded at CERN’s “Bondlab and Quality Assurance Lab” (building 186) by Ian McGill and Florentina Manolescu. For that a work request form available at http://bondlab–qa.web.cern.ch/bondlab–qa/bondlabhome.html had to be filled out. The irradiated sensor was wirebonded at the University of Geneva.
HV CMOS eTCT Box

3D View Box Sides numbered

Box with slits Side View (1)

Top View Peltier Cooling Block

Box Lid Top View (3)

Figure 8: Dimensions of the detector box
Figure 9: Dimensions of the detector box
5 Designing the PCB

5.1 Introduction to EAGLE and PCBs

Printed Circuit Boards (PCBs) are mechanical structures that connect electrical components with each other using conductive tracks. EAGLE ( Easily Applicable Graphical Layout Editor) is a CAD software program to design PCBs. It consists of two parts: Firstly the required electronic parts like resistors, capacitors and connectors are added and schematically connected using the "schematic" view (see figure 10).

![Figure 10: The final schematic for the PCB designed for this investigation. An EAGLE schematic shows the functionality of a PCB. By giving connections the same name an electrical connection is set up.](image)

Once the schematic and the functionality of the PCB has been established, the connections and parts have to be arranged in 2D. This is done with the "board" file where the components are moved around and connected using the wiring tool (see figure 11). Connections that are yet to be made are shown in yellow and are called air wires.

This PCB has been designed as to support both the HVCMOS version 2 and 3 chips. It was important to leave an area free of parts behind the diode, so that the incoming laser would not reflect off them and affect the signal. In fact, in the first measurements a reflection off the side wall of the PCB was observed, that could be avoided by darkening this side wall with a black marker pen.
Figure 11: An EAGLE board file shows the positioning of the electronic parts and connections in 2D. By naming wires the same an electrical connection is established.
5.2 Tips and Tricks for using EAGLE

Later measurements revealed that there were reflections distorting the signal. Paying attention to the length of tracks and performing impedance matching might give more satisfactory results.

To connect two paths in different layers a "via" is needed, that are the holes through the PCB that are marked green in figure 11. However, one can start drawing a connection and then once the first part of the connection is confirmed change the layer. This way a via is created automatically.

Sometimes it is difficult to see a remaining air wire. In order to find it one can zoom out until the board only occupies a centimetre on the screen. Then, one uses the routing tool and clicks on the board. The program selects the first air wire a certain area around the mouse when the user clicks with the routing tool. If this area encompasses the whole board, chances are high, that the missing air wire will be selected.

5.3 Weaknesses of the PCB and hardware hacks

In the end the resistor R2 and the two capacitors C5 and C7 were taken off the board again, because otherwise no eTCT measurement could be performed in the HV branch. The gap left after removing R2 was bridged using the leg of an unused through-hole capacitor. The spots of the capacitors was left empty, so that no current could flow between SUBSTRATE and GND. Two SMA connectors were designed to be on top and two on the bottom due to a misunderstanding. These should all be put on one side for future PCBs.

6 Analysis software

Taking measurements had been automated using LabVIEW. The resulting data files were turned into root files with a custom made script called edge_tree_devel and then analysed with root. A root macro called LoadAll.cxx was written to load all necessary libraries no matter what directory root was opened in. In order to provide documentations for future users of the setup the analysis steps were summarised as instructions:


- Transfer your file from the eTCT computer to your analysis computer using WinSCP. Then connect to that analysis computer by typing the following line into your terminal:

  `ssh -X ssd@pcssd30`

- Change directory to where your data is and put the LoadAll.cxx script into this folder. You can set a path like $SDATA in .bashrc.

  `cd $SDATA`
7  EXPLANATION OF VARIABLES

• Turn the ASCII file into a root file. The file name after edge_tree.devel should be changed to the name of your file.

  –  edge_tree.devel 2014091115854_HVCMOSv3_unirrad.ZVscan

• Open the generated root file.

  –  root -l 2014091115854_HVCMOSv3_unirrad.ZVscan.root

• Load the necessary libraries (if necessary).

  –  .x LoadAll.cxx

• If an error occurs, you might have to open the macro and change the file paths to where your libraries like TMeas.cpp are. Then get the tree of your file

Once all the necessary preliminary work was done, the results could be analysed following these instructions:

• tree– > Draw("volt - BlineMean:time","Vbias== -40 && z==5.13","l")
• plot2D("time:z:volt-BlineMean","Vbias== -20","2014_HVCMOSv3_unirrad.ZVscan.root")
• plot2D("x:z:Sum$((volt-BlineMean) * (time>6.7 && time<9.7))","","2014_HVCMOS.XZscan.root")
• plot2D("y:z:Sum$((volt-BlineMean) * (time>6.7 && time<9.7))","","2014_HVCMOS.YZscan.root")
• plot2D("Vbias:z:Sum$((volt-BlineMean) )","","2014_HVCMOSv3_irrad2.ZVscan.root")
• tree– > Draw("Itot:Vbias","","profy")

7  Explanation of variables

tree  A structure that holds the measurement’s information
volt  The signal voltage
BlineMean  The results of all measurements under one position and bias voltage are averaged and the Baseline extracted
x,y,z  Positions as described in section 3.2
Vbias  Bias voltage applied to the sample
Itot  Total leakage current
8 Measurements

The chip didn’t only feature the investigated test diode, but also pixel matrices and measurement were taken in two different configurations. In the first configuration the signal was measured in the HV branch using only the connections SUBSTRATE and GND (see figure 12). Applying a bias voltage depleted the whole chip rather than the section just below the diode. Signals could be recorded from several parts of the chip making it easier to find the chip.

Once the chip was found, the wiring was changed to configuration 2 described in figure 13. The connection DioNW gave access to the diode itself and could therefore be used to characterise this passive diode directly.

Figure 12: Circuit diagram for the first configuration

Figure 13: Circuit diagram for the second configuration
9 RESULTS

Signals consisted of a "fast" and a "slow" contribution. Anything before 3 ns after the start of the signal was called "fast" in this investigation. Anything after these 3 ns that was called "slow". Some signals had a bigger fast contribution. Others had a bigger slow contribution as shown in figure 14.

![Figure 14: Different shape of signals](image)

There was a lack of clarity of the signal due to the amplifiers and reflections on the connectors and the PCB, which we will try to reduce. However, the peak 50 ns seconds after the start of the signal could be explained, as this was the delay time for a reflection of the primary peak on the 5 m cable that was used. The fast peak was interpreted to be due to drift, while the slower signal was taken to be due to diffusion. The signal minus the baseline integrated over 3 ns was referred to as "quick charge", while the signal minus baseline integrated for 74 ns after the fast signal was called "slow charge".

9.1 XZ

For both the unirradiated and irradiated sample (figure 15), the active region of fast charge of the chip was slightly bigger than the width of the diode (100 µm). This region was interpreted to be the depletion region and had similar properties in both cases.

For slow charge and the unirradiated sample, there was a distinct slow signal of the same order of magnitude as the quick signal. For the irradiated sample no such signal was observed as shown in figure 16. In fact in the centre of the quick charge region the signals of the unirradiated and irradiated sample look similar (see figure 17 ). The slow charge part of the signal was slightly more prominent in the unirradiated case, but the troughs were of comparable size. The two positive spikes in figure 16b were interpreted as being artefact reflections of very high signals because of the high field strength due to the guard ring being on negative high voltage.

When the HV2FEI4v3 sensor was irradiated its slow signal was reduced by an order of magnitude. A possible explanation could be trapping of charge carriers with expected mean lifetimes before
Figure 15: Quick charge which is the voltage minus the baseline integrated over the first 3 ns of the signal

(a) Unirradiated

(b) Irradiated

Figure 16: Slow signal

(a) Unirradiated

(b) Irradiated

Figure 17: Shape of the irradiated and unirradiated signal in the zone of quick charge
trapping in the ns regime. The fast signal, however, did not lose significant height in the conditions considered.

9.2 ZV

To see the dependence of quick and slow charge on bias voltage figures 18 and 19 were drawn. Bias voltage magnitude increased to the left in these graphs. The quick charge zone increased with bias magnitude. The width of a zone over 1 mV was 35 µm for the unirradiated and 40 µm for the irradiated sample. However, there were more steps per µm in z for the irradiated sample and the laser had a gaussian form of 8 µm producing a convolution. Therefore, the actual corresponding depletion regions are expected to be smaller. The irradiated quick charge at 0 V was at least an order of magnitude smaller than the unirradiated one in this case.

<table>
<thead>
<tr>
<th>Vbias</th>
</tr>
</thead>
<tbody>
<tr>
<td>-60</td>
</tr>
<tr>
<td>-50</td>
</tr>
<tr>
<td>-40</td>
</tr>
<tr>
<td>-30</td>
</tr>
<tr>
<td>-20</td>
</tr>
<tr>
<td>-10</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

-z

-5.06
-5.04
-5.02
-5
-4.98
-4.96
-4.94
-4.92

(a) Unirradiated

(b) Irradiated

Figure 18: Fast signal dependence on bias voltage

For the unirradiated sample the slow charge region remained constant in size, but was shifted down by a growing quick charge region. The irradiated sample had the same shape, but the signal was significantly smaller. The quick charge of the sensor at no bias voltage seems to have been due to diffusion and was reduced when irradiated. Radiation did not change the thickness of the depletion region (see figure 20).

9.3 Leakage current and breakdown

At room temperature the current of the unirradiated sample was of the order of 0.3 nA (see figure 21), while it was of the order of 5 µA for the irradiated chip. The unirradiated sensor broke down at 93 V, where its leakage current went over 1 µA. The irradiated sensor broke down at approximately 95 V, where the leakage current went over 10 µA. Cooling reduced the leakage current as expected.
9.3 Leakage current and breakdown

RESULTS

![Figure 19: Slow signal](image)

Figure 19: Slow signal

![Figure 20: Effect of radiation on quick charge zone](image)

Figure 20: Effect of radiation on quick charge zone

![Figure 21: Leakage current is plotted against the voltage.](image)

Figure 21: Leakage current is plotted against the voltage.
10 Conclusion

In summary, it was shown that the signals of the passive test diodes of HV2FEI4v3 sensors had slow and fast contributions. When irradiated, the magnitude of the slow contributions was reduced significantly, while the faster signal contribution remained at the same order of magnitude. Allegations that most of the chip’s signal is due to slow contributions that disappear with irradiation can be rejected.

Furthermore, it was shown that increasing the bias voltage increased the thickness of the quick charge region, which was expected for a functional diode. What was interpreted as the depletion region was measured to be of the order of 20 µm thick. Literature predicts an 8 µm depletion region for 10 Ω cm, so this project’s report’s results seem reasonable considering there was a convolution of the depletion region with a laser of roughly gaussian shape and a sigma of 8.8 µm. However, this measurement was only a rough estimate due to the convolution with the laser used for measuring the thickness.

11 Acknowledgements

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