The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of AIDA Work Package 3: Microelectronics and interconnection technology.

The electronic version of this AIDA Publication is available via the AIDA web site [http://cern.ch/aida] or on the CERN Document Server at the following URL: [http://cdsweb.cern.ch/search?p=AIDA-D3.2]
Abstract:
Wafers with ASIC readout chips suited for 3D interconnection are available. They will be used with high resistivity, fully depleted pixel sensors with different pixel size and pitch. This report gives a short description of the chips and of the interconnection technologies that will be tested.
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The Advanced European Infrastructures for Detectors at Accelerators (AIDA) is a project co-funded by the European Commission under FP7 Research Infrastructures, grant agreement no 262025. AIDA began in February 2011 and will run for 4 years.

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Executive summary

The master plan for the production of demonstrator sensors in 3D technology has been created.

Several subprojects have been defined, each using a different approach of 3D technology and working with different industrial partners.

The subprojects sample technological approaches which range from ‘mature’ (available for production at low risk without important R&D, however with moderate performance) to ‘challenging’ (need of R&D with high risk, but having the potential to reach superior performance). Thus a knowledge pool of different technologies and their respective usefulness and potential for HEP applications will be created.

The partners of this work package are grouped into the different subprojects allowing an efficient use of resources.

1. INTRODUCTION

The main objective of AIDA WP3 is the demonstration of the feasibility of 3D interconnection for applications in Particle Physics. This is the basic goal of task WP3.2, and will be achieved by the fabrication of pixel detectors and readout electronics, interconnected by advanced 3D integration technologies. The knowledge gained with the construction of these demonstrators can be used to design and fabricate detectors for specific applications in particle physics.

This document discusses the status of the dedicated ASICs that the WP3 subprojects have developed as a key element for the construction of demonstrators. As discussed in the following, full wafers with 3D-compatible ASICs are already available to some subprojects, as they were developed in the frame of other large experiments or collaborations. These chips are based on 130nm CMOS processes, or even on technologies with larger feature sizes. On the other hand, WP3 also pursues more aggressive (and risky) solutions, such as 65nm CMOS and 3D CMOS, which are expected to provide full wafers at a later stage of the AIDA project.
2. READOUT CHIPS IN WP3 SUBPROJECTS

2.1. PLANS OF SUB-PROJECTS FOR CMOS READOUT CHIPS

- **Bonn/CPPM**: Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).
- **CERN**: Interconnection of MEDIPIX3 chips using the CEA-LETI process.
- **INFN/IPHC-IRFU**: Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others).
- **LAL/LAPP/LPNHE/MPP**: Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.
- **MPP/GLA/LAL/LIV/LPNHE**: Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.
- **RAL/UPPSALA**: Integration of a 2-Tier readout ASIC for a CZT pixel sensor using EMFT SLID technology and TSV including redistribution of I/O connections to the backside for a 4-side buttable device.

For a more details description of these WP3 subprojects, the report for Deliverable 3.1 can be used as a reference.

2.1.1. Bonn/CPPM

The goal of this activity is to develop a 3D integration technology applicable to the innermost pixel layer of the detector at High Luminosity LHC. Within the AIDA R&D framework WP3, we propose to produce real chip/sensor assemblies to test an interconnection technique allowing the access to the wire bond pads of the 3D structures after bonding.

For these prototypes, we propose to use planar ATLAS pixel sensor wafers and the ATLAS pixel FE-I4 electronic chip wafers. The FE-I4 chip [1] contains readout circuitry of 26880 hybrid pixels in 80 columns by 336 rows and it is produced in the 0.13 µm feature size bulk CMOS process by IBM. The pixel pitch in FE-I4 is 50x250 µm. The dimensions, 20x19 mm², are the biggest among HEP chips and close to the maximum size allowed by most of the vendors. The backside wire bond pad access by means of via will allow mounting two (or four) chip modules with the sensor side on the mechanical-cooling carbon structure.

Three wafers of the FE-I4A chip are available and will be used for a first run of TSV fabrication.

First wafers of FE-I4B ICs are reserved for ATLAS Insertable B-Layer project. When FE-I4B wafers become available, we plan to buy some, as well as planar sensor wafers and ship to IZM and/or LETI where post-processing will occur. Access to FE-I4B backside through wire-bonding to a potential backside redistribution layer can be done in-house in Bonn. Process evaluation based on Bonn/CPPM experience with standard FE-I4B will be performed in both labs.
2.1.2. CERN
The proposed project uses Medipix3 read out chips [2] as the platform for 3D integration development. The aim of the project is to utilize an existing mature TSV technology made available by CEA-LETI as a part of their open 3D initiative. Medipix3 wafers are available, and TSVs tests were already successfully performed.

2.1.3. INFN/IPHC-IRFU
The goal of the INFN/IPHC-IRFU proposal in the framework of the AIDA WP3 is the design and fabrication of a multi-tier pixel sensor resulting from the vertical interconnection of a CMOS readout circuit to a separate CMOS layer optimized for particle sensing and to a fully depleted edgeless or 3D detector. The project relies on CMOS sensors designed by IPHC-IRFU, fully depleted detectors provided by FBK Trento and a mixed signal readout chip designed by INFN.

The readout chip is foreseen to consist of a dual-tier mixed signal circuit fabricated in the Tezzaron/Globalfoundries vertical integration CMOS technology, where each tier is based on a 130 nm process.

Actually, some of the proponents are already working on the design of a readout chip for hybrid pixel detectors in the 3D 130 nm CMOS process provided by Tezzaron/Globalfoundries [3]. This activity is carried out again in the framework of the VIPIX INFN experiment. This chip may be used also for the readout of CMOS sensors; in this case, an amplifying stage with an adequate gain has to be integrated in the sensing layer to account for the smaller signal that is expected with respect to a typical fully-depleted, high resistivity sensor. This 3D chip is planned to be submitted by the end of 2012, and should be available in 3Q 2013.

2.1.4. LAL/LAPP/LPNHE/MPP
This subproject plans to exploit the challenging 65 nm CMOS IBM technology to build a single electronic layer that houses both analogue and digital parts, interconnected to a sensor layer using via last and SLID innovative technology. This approach is similar to another proposed subproject using ATLAS FEI4 readout circuit and some synergy will be achieved in terms of SLID evaluation and electrical tests.

The availability of 65nm design tools for use in our laboratories for our application in high energy physics combined to novel 3D interconnect technology will create a new generation of advanced devices to increase the density, and minimize the space and power consumption.

Experimenting this kind of challenging technology thanks to the AIDA support, in a collaborative partnership sharing the knowledge between high energy physics European laboratories (CNRS, CERN, INFN, MPI…), and also with industries (pioneering firms, IBM, VTT, EMFT…), could speed up the migration of the knowledge from the actual 130 nm 2D design to the more challenging 65nm electronic readout associated with 3D interconnect
technology. A first 65nm demonstrator ASIC pixel readout circuit is scheduled for the end of 2013.

2.1.5. MPP/GLA/LAL/LIV/LPNHE

This activity regards the interconnection of the new FE-I4 ATLAS chip, designed for the upgrades of the ATLAS pixel system, to a compatible sensor by using 3D technologies developed by the Fraunhofer Institute EMFT. We will use the FE-I4 chip in this demonstrator because it is one of the last generation read-out chips for pixel sensors in high energy physics and it will probably evolve in the following years into a 3D compliant version, for the future upgrades of the ATLAS pixel system beyond IBL. The post-processing for this vertical integration technology has to be performed at wafer level. The availability of full chip wafers is therefore mandatory.

Three FE-I4 ASIC wafers have been ordered within a common ATLAS production at IBM to fulfill the ASIC needs for IBL and R&D activities beyond Phase I. Each wafer contains 56 FE-I4 chips. The chip from two of these wafers will be used for the interconnection to the pixel sensors while one will be dedicated to the development phase of our R&D activity. As main target of this project we aim to achieve working FE-I4 chips with TSV at the location of the original wire bonding pads, with the read-out performed through the back-side fan-out.

2.1.6. RAL/Uppsala

These partners will look at two activities: one is for the construction of a full 3DIC stacked pixel ASIC with pixels interconnected between 2 layers, and the second is for an activity to redistribute I/O connections to the back of an ASIC to enable 4-side butted pixel detectors.

A 40 x 40 pixel readout ASIC has been built based on an existing 80 x 80 pixel Hexitec CZT readout circuitry [4]. The Analogue pixel circuitry is exactly the same as the Hexitec ASICs which are successfully being used. The second digital layer contains a run-down ADC in each pixel and the digital readout circuitry necessary from this layer. There is one TSV interconnect from the analogue pixel on the top layer to the digital on the bottom layer and one for each I/O connection as all readout is from the top layer. Both devices have been built and tested in previous years and the 8 wafers of devices have been supplied to EMFT Munich for integration.
3. CONCLUSION

This document presented a summary (see also Table 1) of the plans that AIDA WP3 will pursue with the goal of procuring CMOS wafers with readout chips in view of the fabrication of pixel detector demonstrators based on 3D integration. Wafers with chips from the ATLAS and Medipix collaborations are already available, and tests of 3D integration features are under way. The same is true for the readout ASICs that the RAL/Uppsala subproject is using for its demonstrators. Other subprojects, namely, INFN/IPHC-IRFU and LAL/LAPP/LPNHE/MPP, are planning to design and fabricate new chips, respectively in the 3D-IC technology by Tezzaron/GlobalFoundries and in a 65 nm CMOS process. These chip prototypes are expected to be available in 2013, allowing the subprojects to build 3D demonstrators in the AIDA time frame. A short annex will be added to this deliverable when these wafers are available for these last two projects.

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<td>RAL/Uppsala</td>
<td>Hexitec (CMOS 350 nm)</td>
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Table 1. Summary of the ASIC availability for the fabrication of 3D pixel demonstrators.
4. REFERENCES


