Delivering VLSI chips to HEP experiments

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1. ABSTRACT

This paper discusses some of the lessons learned in recent years by participating to and observing design projects in microelectronics for the LHC. The perspectives and implications opened up by the continuous enlargement of the portfolios of microelectronics technologies offered by the silicon foundries are also presented.

2. DISCLAIMER

This paper reviews the history of the last few years of activity of a major part of the HEP electronics design community and may therefore be the only paper presented at this conference without a distinct technical or scientific content. The aim is to point out those areas of our organization that need improvement. Such improvements will be necessary to provide future generations of physics experiments with the instrumentation for improved detectors at a cost and within delays that are affordable by our community.

3. INTRODUCTION

The need during the first phase of construction of LHC experiments to have access to a low-cost, high quality technology with extreme radiation tolerance characteristics has pushed our community to set up an in-house Multi-Project-Wafer (MPW) service which has supported designers with the means to develop and manufacture almost one hundred different integrated circuit designs. These range from high volume (on our relative scale), cost sensitive front-end read-out chips, to very low volume, extremely dedicated chips, in which the entire project cost is dominated by the engineering development.

Although it is unlikely that the coming years will demand a similar effort as regards quantity of chips and number of designs, it is now clear that Application Specific Integrated Circuits (ASICs) are becoming a de-facto asset in HEP instrumentation. The HEP community is unlikely to abandon its large investment in the ASIC development capability that it has painstakingly acquired in order to meet the challenges of the LHC project. In the future the community will certainly need to refine, upgrade, optimize and improve existing detectors and this will definitely require the design and production of new ASICs.

In parallel, and despite numerous gloomy predictions, microelectronics industry still marches forward at the pace of Moore’s Law. More advanced and sophisticated technologies are being introduced in fabrication lines all over the world, and the benefits these bring can be very significant also for HEP applications. This evolution would be straightforward if the costs remained constant, but while new technical challenges related to the introduction of even finer technologies are appearing on the horizon, the costs of mask making for newer technologies are expected to escalate significantly.

Based on the experience which was gained in running this service in the past years, and having learned from the mistakes sometimes made, our community will likely need to put in place a renewed service capable of offering access to newer technology in a smooth and affordable way.

While prototyping could be well supported by existing organizations such as Europractice and Mosis, the production of large series and debugging of complex chips can only be successful if a competent support service remains available within the community.

4. BACKGROUND

The four LHC experiments represent possibly the largest-ever non-military application of radiation-tolerant ASICs. While comparable in complexity and reliability requirements with applications such as space and avionics, the volume of electronics channels required by HEP applications surpasses by at least a few orders of magnitudes (in terms of chip count, but certainly not of dollars) those markets. As examples we will use the CMS central tracker detector, needing some 100,000 front-end ASICs and some 20,000 service chips. The electromagnetic calorimeter in the same experiment is even more demanding, with twice 80,000 front-end chips and about another 30,000 service ASICs. In parallel, the Atlas, LHCb, Alice and CMS collaborations are all designing some extremely complex pixel detector ASICs, where – although volumes are relatively modest on a commercial scale, as some 10,000 chips are needed per experiment – the analog complexity of these ASICs is totally unprecedented in HEP. For a summary of the production volumes for quarter micron chips for LHC and the number of design iterations see the Figure 1 below.

It is perhaps worth stressing at this point that, while it is the extreme environmental conditions of the LHC that have imposed the design of radiation-tolerant ASICs, the architecture and requirements of future HEP detectors will continue to demand the design of dedicated integrated circuits, because no suitable off-the-shelf commercial chips will be available for the front-end applications.
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sub-micron process. This paper only covers the history of use both a “military-grade” radiation-hardened (but less tolerant characteristics justified an intense R&D period in the 1990’s, where many Institutes in Europe and the USA, coordinated by CERN’s Detector Research and Development Committee (DRDC, for a list of approved projects see [1]) and similar programs, explored potential solutions along different technology and commercial routes. The LHC design era has profited from the on-going exponential growth of the microelectronics industry, and - in particular - with the introduction of the first deep sub-micron technologies. As amply documented elsewhere [1], the thin gate oxides used from the 0.25 um generation from the late 90’s onward have offered an almost miraculous solution to the difficult problem of the voltage shifts generated in MOS devices by the trapping of charge in the oxides of previous generations of technologies. What previously required expensive and proprietary radiation-hardened technologies could now be tackled with some clever layout techniques and the benefits of low-cost mass-produced technologies.

Considering that the introduction of the quarter micron technologies in industry occurred just at the time when the LHC was initially expected to become operational (around 1997), our community adopted a cautious approach of using both a “military-grade” radiation-hardened (but less lithographically advanced) technology, and an advanced deep sub-micron process. This paper only covers the history of use of a quarter-micron feature technology.

5. OBSERVATIONS FROM THE POSITION OF A SERVICE PROVIDER

The demand for low-cost chips with enhanced radiation tolerant characteristics justified an intense R&D period in the 1990’s, where many Institutes in Europe and the USA, coordinated by CERN’s Detector Research and Development Committee (DRDC, for a list of approved projects see [1]) and similar programs, explored potential solutions along different technology and commercial routes. The LHC design era has profited from the on-going exponential growth of the microelectronics industry, and - in particular - with the introduction of the first deep sub-micron technologies. As amply documented elsewhere [1], the thin gate oxides used from the 0.25 um generation from the late 90’s onward have offered an almost miraculous solution to the difficult problem of the voltage shifts generated in MOS devices by the trapping of charge in the oxides of previous generations of technologies. What previously required expensive and proprietary radiation-hardened technologies could now be tackled with some clever layout techniques and the benefits of low-cost mass-produced technologies.

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- Qualified design tools: mainly a cell library, validated simulation models, a Design Rule Checker (DRC) deck, and a complete design flow methodology.
- A reasonably regular MPW service: a service to assemble reticles containing multiple designs for submission to the foundry, a final design checking service, an interface with the foundry, engineering support for those designs (and there were many in our community) for whom the foundry design manual did not satisfy the insatiable technical curiosity of our engineers.
- Logistic and accessory services: for instance wafer dicing, prototype packaging, integrated circuit testing.
- Some engineering support for new users wishing to embark on designs using this technology.
- Commercial and legal framework contracts satisfying both the complex and intricate rules and constraints governing procurement by an international organization and the needs of the users in the community.

The reader can easily discern that, as in any service organization, managing an MPW support organization can be extremely rewarding, and honestly sometimes also a little frustrating. A number of lessons learned from this experience can be drawn and hopefully be used to minimize such frustrations in the future.

5.1. Libraries

As already practiced in software projects since many years, the efficiency of a designer can be greatly enhanced by providing him/her with a set of predefined library elements that can be easily used to construct a design using a synthesis tool (analogous to the use of a compiler in high-level language programming). The requirement for special layout techniques and the restricted manpower resources available limited our digital library to some two dozen logic cells and a minimum number of IO cells (for comparison, a commercial library typically consists of several hundred core cells and many tens of IO cells). The great majority of digital designs also need high density storage, typically implemented with static Ram cells (SRAM). Our limited resources have been able to produce only a set of primitive cells that can be assembled manually to produce a full single- or dual-ported SRAM of configurable size.

Characterization of the library is also an area where far more work will be needed in the future. For designs of more than 50-100,000 cells, the speed of ASICs realized in quarter micron CMOS and below is dictated by the wiring parasitics of the chip and not by the intrinsic gate delays. Extracting a proper statistical model of the wiring of our chips is still an unfinished task and much heuristic and experience-based guess-work has been put in the current generation of large digital ASICs, even to run at the rather modest digital speed of 40 MHz. The proper construction of clock trees and respect

![Figure 1 Number of iteration cycles and production volume for various chip design projects.](image-url)
of hold time constraints of flip-flops in large chips require more sophisticated signal integrity analysis tools, even when the cycle time is much less than the maximum the technology could theoretically support.

Analog designers come characteristically very close to true artists. They pay (and they very often have to) enormous attention to the detail and dislike reusing previous cells or – worse – cells coming from other artists. Nevertheless, the availability of a number of basic cells in an analog library would have significantly and measurably accelerated the design of certain projects, and also diminished their risk. While the concept of analog library still maps to an almost empty set, a future analog library should be composed minimally of:

- Voltage and current parametrizable reference cells.
- Bread-and-butter operational amplifiers.
- Low resolution or low speed but readily available DACs and ADCs.
- A set of computational tools capable of calculating analog cells based on a true mathematical optimization of a model of the cell, more than the prevalent approach of design by iterations that is largely applied in our analog design community.
- As recent experience has finally shown, extraction of layout parasitics (wire resistance and cross-coupling capacitances) has to be present early in the layout phase, so as to avoid extremely tricky and treacherous pitfalls and mistakes. Such parasitic elements must be fed-back into the Spice or timing models automatically.

5.2. Tools

It is a fact of life that the enormous advantages offered by high density modern technologies can only be mastered when the appropriate design tools are available. As an example, the design of pixel front-end chips is greatly facilitated by high density, multi-metal layer technologies, but the extraction of parasitic effects from these high density layouts demands the most performant and modern tools. Unfortunately these tools are perceived as “luxury” items in our community and amazingly all sorts of excuses are invented to justify why we can do without them, often instead compromising the quality and the performance of the resulting chips. Designs have failed and expensive resubmissions have occurred because of the rather primitive status of the extraction tools that have failed to prevent – for instance – the submission of chips with unreasonably long wires or unreasonable loads on certain signals. Although industry offers power analysis and optimization tools, our community has not been willing or able to use them, and tricky issues such as metal electromigration and in general chip reliability have often been underestimated or neglected. The HEP Management at large is easily spending large (but not readily accountable) resources in Monte-Carlo simulation tools for the physics of the experiments, but becomes immediately extremely reactive if a smaller (but explicit) amount is requested for a set of advanced commercial design tools.

Voltage drop on (slightly) resistive lines, substrate coupling, signal cross-coupling and systematic full corner simulations would all require more sophisticated tools than those that have been used in the first LHC design generation. Voltage drop on power lines during high current consumption periods brought an otherwise successful design very close to disaster, when it was realized that the chip could grossly malfunction due to this effect. This problem could fortunately be fixed with a modification of two metal mask layers, but it had a significant impact on the project schedule. The appropriate analysis tools that would identify these problems are commercially available, but apparently not affordable by our community. At the same time, designers need to be better educated to take into account through these tools all the non-idealities that accompany a real ASIC fabricated on a real production line. This can be achieved by making systematic design reviews more common.

Finally, to the best of my knowledge, no hardware software co-design has been seriously attempted and often entire read-out chains have been designed and built without the benefit of any system level simulations.

5.2.1. Testing and verification tools

It is certainly true that the ultimate proof of the applicability of an ASIC for a given experiment is a final verification in a test-beam. On the other hand, given the high cost and additional complexity of such a validation procedure, much more should typically be done on well-controlled test-benches, and especially on parametric IC testers. A validation in a test beam provides certainty that the electronic chain would work under the conditions implemented in the given setup, but actually provides no useful information on the margins available on a given ASIC in terms of timing, temperature and voltage parameters. It also does not generate the parameters that are typically used to characterize commercial components, such as bandwidth, signal distortion, precise robustness to power supply noise, electrical noise margins and timing margins. The investment in parametric IC testers has been made by very few groups in our community.

In terms of production testing, while most commercial circuits of considerable complexity are tested in a matter of a few seconds, it is not unusual that our ASICs require many tens of seconds, if not minutes to be tested. Tester time is precious, and this indicates clearly that often not enough effort has been spent at the design time to include testability in these ASICs, or at least to include features that would reduce these unrewarding and costly tasks to much shorter durations.

5.3. Organization of MPW runs

Modern CMOS technologies can make very powerful chips thanks to the large number of options that technologists in semiconductor foundries have built into them. A number of metals, device options, analog options and even passivation
options have to be agreed upon by everybody when accessing an MPW service. The large size of the choice-space can leave many people unhappy when options have to be accepted and paid by everybody. Restricting everybody to a single set of options is unfortunately the only economically viable solution, but can generate incomprehension and unhappiness in some users. A typical example is the pixel design groups, who often require all the metallization options offered in a technology, while other cost-sensitive front-end designs can easily be routed with many fewer metal layers.

An example of a reticle assembled for sharing prototyping costs on an MPW run with about 20 designs is shown below.

Figure 2 A typical reticle for an MPW run

5.4. Relationship with foundries

Two types of relationships have to be organized and maintained: the first at the commercial and strategic level, the second at the day-to-day technical level.

5.4.1. Commercial relationship with foundries

Available statistics on production volumes for industrial designs show that on average half of the generated mask sets produce less than 500 wafers[3], which underlines that the enormous volume production capacity in industry (around one million 8” equivalent wafers per week in 2003 [4]) has been justified mainly by the very high volume products, such as DRAMs and microprocessors. The statistics derived from submitting some 200 HEP designs show that very large volumes are not frequently required in our community, and that the number of low-volume designs greatly outnumbers those with a high quantity of chips. This fact constrains us to maintain a very special relationship with foundries. Modern foundries are machines optimized to make (a lot of) money by producing a selected chips in very large quantities. Semiconductor foundries are among the most expensive industrial enterprises in all industrial sectors, with costs approaching the 10 B$ mark per foundry. To be economically viable each of these foundries have to produce thousands of 8”, and in the near future 12”, wafers per day. By comparison, a reasonable estimate of the global need for LHC is below ten thousand wafers over the total construction period of the project.

It is clear that relationships with these foundries therefore have to be seen as strategic elements of the experiments, and all negotiations have to be handled at the appropriate level.

5.4.2. Technical relationship with foundries

It is not new that designers can make mistakes, but large foundries can make mistakes too. The process of manufacturing a typical quarter-micron design requires about 20-24 lithographic masks and some 600 individual process steps. Some of these steps demand process control to be mastered at the level of a few nanometers or better on a 20 cm wafer. Sometimes mistakes are generated by genuine human or machine errors in the production line. Occasionally mistakes are generated also by incorrect interpretation of design rules as design for manufacturability is not included in the hard rules coded in the DRC deck. As a simple example, connecting nodes via metal lines using a single contact or via is allowed, but should be used sparingly as to improve manufacturability of the circuit.

Understanding why one design yields consistently well, whereas another behaves erratically in different production runs can be ignored when the production lots are modest or the design is of academic interest only. However, such issues must be understood quickly for production lots of several hundred wafers. Understanding an apparently random yield behavior can require very sophisticated and expensive equipment and access to the even more precious design and process experts in the foundry. Such access can only be organized if an excellent communication and partnership has been established with the foundry; the required degree of communication largely exceeds the standard supplier-customer relationship for the kind of volumes required by our community.

5.5. From prototype to production

Experience has demonstrated that our community has often been (if not almost totally) unprepared for the delicate moment when circuits working well in small prototype versions are pushed through into production volumes. Surprises occurred essentially because this phase is relatively uninteresting for designers, but is still risky and complex. Understanding what went wrong in production, when the problem at hand is the result of a complex interaction between a specific design and some weak spot in the manufacturing process is a difficult, expensive and very time-consuming task.
that requires full collaboration between the foundry and the
design engineers.

Problems of this kind have occurred in all technologies,
are well known to experienced foundry people and are typically
related to the well-know issue of “design-for-
manufacturability”. Written and unwritten rules exist in this
respect. For instance, any serious industrial design house
would simulate designs for compliance to the project
specifications under all process, voltage and temperature
corners. Relatively few written rules exist about issue related
to layout techniques and the best approach is to organize
design reviews of complex and high volume chips with
experts from the foundry. For the LHC chips this was rarely
done and, to avoid expensive re-spins and related delays,
should be introduced in a more systematic way before any
future large volume tape-outs.

![Figure 3 Example of cross-section of faulty chip](image)

Figure 3 Example of cross-section of faulty chip

Even so such problems will still occur, and it will then be
vital to have immediate access to the competent process
ingineers in the foundry. This would be extremely difficult if
it had to be organized through a generic, third party-run MPW
service providing the interface to the foundry for a wide
spectrum of users from different communities. Design
engineers have to consult with process specialists, because
hunting down a complex design-process generated yield
problem requires both engineers to be present, in addition to
the traditional test engineer. Experienced physical analysis
people are also required, as the interpretation of data and
images from measurements and electron microscopy is not
obvious for the average design engineer. A typical cross
section of a faulty area of a chip is shown in Figure 3 above.
In addition, the foundry specialist has the experience
necessary to understand whether a proposed explanation for a
problem is reasonable or not. Once again, direct
communication with the foundry is necessary for all projects
where quantities are large. From our experience, the solution
of one specific but complex yield-related problem required
more than 6 man-months on our side, and possibly twice as
much on the foundry side.

5.6. **Size and structure of design groups**

Although potentially controversial, some observations
must be made concerning the structure of the groups
designing ASICs in our community. The prevalent model for
the industrial engineer is the horizontal one, where each
individual is stressed to the largest possible extent in the
direction of specialization in accomplishing a single function.
In contrast the HEP community – certainly out of necessity –
works with deeply vertical engineers. People are asked
consistently to participate to the design specifications, the
design implementation, the design debugging, testing and
finally to the installation in the experiment. This is to be
compared to professional chip design companies, where even
the task of making a layout is considered a “lower-level” job
and is not performed by the engineer, but by technicians.

While the universal engineer (or physicists) is an almost
untouchable truism of our community, its measurable
efficiency is still to be proved. Often this leads to sub-critical
mass design groups, in which single individuals have to
handle an entire complex electronics project instead of the
design of an ASIC. Design times are extremely long because
all phases of a project are serialized by construction through
one person (a single person can only perform one job at a
time). It is even quite common in our community for a single
ingineer to act as the principle engineer for two or more
designs concurrently. It is now quite clear and undisputable
that time-to-market (in our language: “time-to-experiment”)
could be greatly improved by having less projects and more
people per design. Several groups have experienced projects
in which the design time was so long that the preferred
technology selected at the start of the project became obsolete
towards the end, or even the project had to be transferred to
another technology. We also had cases where a project had to
be completely overhauled because the single project engineer
allocated to it for some reason left for another job.

Long development cycles mean also high (hidden)
development costs. Optimizing the design cycles through the
allocation of proper engineering resources on each project
could also be advantageous in this respect.

6. **CHALLENGES FOR A FUTURE ASIC DESIGN SERVICE**

VLSI design was started in our community as an R&D
activity and was regarded as a creative engineering task
requiring original thinking. This is certainly true when system
and ASIC architectures have to be defined and even more so
when unexplored territories such as analog memories, high
speed analog optical read-out, or high density pixel detector
architectures have to be explored. On the other hand the
production and support roles require typically a very different
profile for the people involved, and therefore an adjustment
might be necessary. Some projects also naturally go through
different phases: at the beginning very different and
innovative architectures are explored and tried and some of
them might survive this selection period. In a second phase
some projects become more evolutionary, rather than
revolutionary and the profile of the engineers allocated to the project might need to be changed. Continuous improvement is still necessary and funds to go beyond the phase where the chips are “just enough” for the experiment should be considered. The investment for continuous education of an affordable number of design engineers should be preserved.

6.1. New technologies for future experiments

The main part of the paper has been dedicated to a review of the experience gained with providing an MPW service with what is today a well-established technology. This last section of the paper will discuss the problems expected if the need for a more advanced technology is confirmed in the near future and it makes some practical proposals on how to organize the community for accessing more advanced technologies under conditions which are hopefully technically and financially affordable. For a review of the expected developments in industry see Ref [5].

6.2. Utilization of 130 nm technologies and below

The beneficial transition to the quarter-micron technology for LHC chips does not need to be stressed again here. From a technical standpoint perhaps this can be summarized with the large amount of low power circuitry than can be squeezed in a few millimeters squares. However, assuming that the environmental conditions of a future generation of HEP experiments will be equivalent to, or not easier than, those at the LHC, then microelectronics for instrumentation will have to address a number of new challenges, mainly, but certainly not exclusively, as follows:

- The reduction of power in front-end channels. This is perhaps the single most difficult task because it requires an integrated approach in which technology, circuit design and architecture will all play an important role. If detectors with higher granularity are to be developed in the future, the power consumption per channel has to be reduced by the corresponding amount.
- The availability of low cost service or auxiliary ASICs for the implementation of complex systems. For instance, it appears uneconomical to have a number of different slow-control systems all essentially doing the same or very similar jobs when one well-engineered solution could satisfy all requirements.
- A common approach to the distribution of fast signals in the experiment. This has perhaps been the single common ASIC development for the first generation of LHC, but it took so long to have it on the field that by the time the last chip was packaged, the manufacturing line has been closed down leaving us with an uncertain future.

Even in the situation where the environment will allow the use of standard off-the-shelf commercial components, there will still be the need for ASICs which are very specific to particle physics instrumentation, such as front-end low-noise charge-sensitive amplifiers, pipelined multi-channel read-out ASICs with analog memories for silicon detectors, high resolution time to digital converters, fully integrated signal amplification, digitization and digital signal processing chains used in calorimetric applications and many others. For instance, the availability of a bank of integrated analog to digital converters together with dense digital circuitry to perform extensive digital signal processing on the data has been shown to be extremely beneficial in the Altro chip [7] in Alice. A 130 nm technology would allow the design of a second generation of channel processing ASICs such as this one, with considerably more logic, and where a high speed serializer and a full slow-control interface could be integrated to substantially reduce system cost.

For the applications mentioned above, the 130 nm CMOS and finer generations could easily offer benefits over today’s technologies as it allows even more data processing with less power consumption per computation. For instance, whereas a typical 0.25 µm inverter gate takes 5.5 µW at 100 MHz, a 130 nm similar gate would consume only 0.58 µW at the same frequency. The scaling of power consumption for the analog front-end stages is unfortunately less obvious and a substantial parallel effort will be necessary to take full advantage of such a technology through original circuit but possibly mainly through architectural innovations.

6.3. Technology choice

The portfolio of process options that foundries offer in advanced CMOS technologies is becoming ever larger - more device types, many metal layers as well as analog- and RF-optimized process variants contribute to the richness of options available to the customer. For example, normal Vt transistors are accompanied by faster low Vt devices for high speed, and devices with thick gate oxides for 3.3 and 5 V IO compatibility. Thus an MPW service can not easily satisfy all users, as the inclusion of unused options for everybody is not free and most designs tend to be content with some minimum sub set of options.

The choice of a new base technology will have to be based on a compromise around the needs of the largest projects, while the more modest ones will inevitably have to accept their choices. However, certain particularly demanding projects, such as the very high-density pixel ASICs, will most likely have to be treated as exceptions.

The option of using BiCMOS devices, with the well-know benefits offered by higher gain bipolar devices will also have to be studied carefully again.

6.4. New challenges for tools

As soon as the semiconductor industry hits the magic 100 nm barrier (this will occur in industry well before the turn-on time of the LHC), new and even more difficult tool problems will have to be faced. Complex capacitive dynamic cross-coupling and inductive effects on chip wires will start to appear, raising again the technical challenges for a new generation of CAE tools in which floor-planning of logic
blocks and signal buses need to be considered early in the design flow.

Purely analog designs are unlikely to grow much in size, but mixed-signal designs are very likely to become much larger, requiring sophisticated signal and substrate analysis tools. Complex Systems-on-Chip of this type can be conceived only with very powerful design tools.

6.5. Organization of services beyond mask submission

The organization of regular user group meetings has proved to be a very effective means of exchanging information in the community and allowing designers to report problems to the service providers and to become acquainted with developments generated in the community. This will have to be extended considerably in the future.

The negotiation of access to a commercial library should also be organized globally, so as to offer the best set of tools at a reasonable cost to users. Companies providing libraries and sophisticated tools are typically uninterested to negotiate with smaller customers, and an approach to serve all designers in the community can only be offered through an in-house effort.

Another often forgotten but essential service is packaging. This is an extremely competitive sector with very small margins and companies operating mainly from the Far-East with low-pay manpower. A central packaging service with a global contract similar to the one organized for silicon wafers would be conceivable and certainly beneficial for the community.

6.6. Wafers cost projections

The current published prices for 180 nm mask sets and the projections for the coming 130 nm generation are sufficiently high to cause distinct concern even in industry. Unfortunately there is apparently no breakthrough to be expected that could bring these high costs down. This fact penalizes particularly the low (and very low) volume projects in HEP, which numerically constitute the majority of the projects (out of 74 projects that have reached “production”, 20 require more than 10,000 parts, 43 more than 2,000, and 6 less than 2,000).

These costs can be maintained within affordable limits through a combination of:

- Reduction of the number of prototyping cycles, that in turn can be achieved through re-usage of common blocks.
- Increase of the number of “clients” using the MPW service, for instance making favorable financial and technical offers to those users in our community who are still accessing other foundries independently.
- Sharing of our MPW runs with non-HEP customers, such as some foundries seem to be willing to offer.

7. Summary

The generation of experiments that will soon run at the LHC machine is possible mainly because sophisticated ASICs could be designed at an affordable cost and in advanced technologies. The massive introduction of dedicated integrated circuits in the detector read-out systems has completely changed the way particle physics experiments are conceived and organized. While ASIC design has been largely a new, unexplored and exciting activity in the first LHC generation, it will become progressively a well-established and pervasive technology in the future. This will require a further “professionalization” of those working in the field as either designers or service providers and a consolidation of the community.

The ever increasing complexity implied by the usage of VLSI technology and the increasing mask making costs will also require an optimization of how designs are developed in our community, both in terms of design team structure and project management. Duplications may no longer be affordable. Overall design time will also have to be shortened and optimized. The small size of many of our project teams must further be strengthened with more effective ways of gratifying collaboration.

A fine balance will have to be achieved in terms of overall system cost/performance ratio, with more aspects of the ASIC design process becoming explicit.

The success of a very visible part of the HEP community will largely be measured in a few years also through the performance and the quality of the ASICs that are today about to be completed and installed for Alice, Atlas, CMS and LHCb.

8. Acknowledgements

Setting up an MPW service at CERN during the last five years required the dedicated work of many individuals. Many people have been working behind the scene to maintain a smooth relationship with the foundry and to provide users with good design tools and verification procedures. Almost the entire MIC Group at CERN has participated with enthusiasm to this effort, but no results would have been achieved without the daily administrative and technical work of Federico Faccio and Giovanni Cervelli. Kostas Kloukinas did most of the initial work for the design and characterization of the digital library and of the SRAM macros, a contribution that everybody today takes for granted. Michael Campbell translated the cryptic Hercules DRC rules into the even more cryptic Diva rules. In addition, the courageous support of Giorgio Stefanini in the early stages of the effort has been fundamental to help us introduce the new technology in an often skeptical and reactive environment. The CAD group at RAL has been instrumental in the early stages with providing us with a professionally built design kit for a quarter-micron technology.
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