The HERA-B electromagnetic pre-trigger and its possible adaptations to the LHC-B Level-0 calorimeter trigger


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Abstract

In this document the pretrigger system developed for the electromagnetic calorimeter of the HERA-B experiment is described, showing some possible implementations of this system to perform the LHC-B Level-0 Trigger for the Electron and Hadron Trigger Algorithms.

1 Introduction

In this document some hardware implementation are proposed for the LHC-B 0 Level electron and hadron trigger based on the design and the experience gained up to now on the HERA-B electron pretrigger.

One of the fundamental common features of the two experiments relevant to design the trigger system is that a lot of information has to be processed but the occupancy per event is low (at the level of 10% or less) like the number of candidates per event.

In the specific case of the HERA-B electromagnetic (em) calorimeter (ECAL)
the main task at pretrigger level is to inspect, by applying a proper algorithm, the full detector acceptance (about 6000 readout channels) to identify an average number of two electromagnetic cluster candidates per bunch crossing (BX). The other HERA-B trigger systems (muon, high-\( p_t \)) have to face the same problem: select a few tracks per BX starting from some \( 10^6 \) “roads” for tracks within the parameter space allowed to the trigger system. To summarize: a large amount of data readout is provided by the detectors involved in the trigger system, but only a small quantity of them have to be processed.

As a consequence of this characteristic, a general strategy has been adopted for the HERA-B first level trigger (FLT) through the following steps: [1]

- **Track seeding**: scanning over all the particle identification (ID) detectors (ECAL, muon, high-\( p_t \)) to find candidates and addressing regions of interest (ROI) in the tracking system. Create from the pretrigger stages *messages* that contain all the relevant track parameter and the address of the ROI.
- **Track finding**: updating (refining) of the messages at each step of a back tracking performed with a Kalman filter inspired algorithm.
- **Trigger decision**: last step for the definition of the track candidates parameters (starting from the messages), and calculation of the physical quantities (masses of pairs, high momentum cuts) necessary to trigger on specific channels.

This strategy allows to limit the number of processors needed by moving processes to data: the processors perform operations only on the small amount of data addressed by the (few) messages. This approach leads to a consistent reduction of the number of processors without loosing trigger algorithm flexibility (data processing is performed by look-up tables (LUT)).

In the following it will be shown first how these aspects have been achieved in the HERA-B electron trigger system: by about one hundred processing units only it is possible to perform all the pretrigger algorithm on electromagnetic clusters on the 6000 ECAL readout channels.

In Section 2 of this document a description of the electron trigger developed for HERA-B will be given; in Section 3 it will be shown how in principle it is possible to adapt the HERA-B electron trigger strategy to the LHC-B Level-0 (L0) electron and hadron trigger.

2 The HERA-B electron trigger

A detailed description of the HERA-B electron trigger can be found in Ref. [2]. Here the main features finalized to a comparison with LHC-B L0 trigger will be reported. In the following we will refere also to the front end driver cards especially designed for the ECAL readout that are fully described in
2.1 The electromagnetic calorimeter and the readout system

The HERA-B electromagnetic calorimeter is a shashlik type one, whose structure is very close to the LHC-B ECAL one. It is divided into three regions (Inner, Middle, Outer) having different granularity in order to get an occupancy uniformly distributed at 10% level. The main structure of the detector is a module consisting in a square cross section calorimeter tower having 11.15 cm side. In the Inner ECAL a module is subdivided in 5x5 readout cells having tungsten as converter and scintillator tiles as active material. Due to the tungsten Molière radius (1.3 cm) an em shower develops itself mainly in one readout cell having about 2.23 cm side. This allows to keep particle pile-up at a reasonable level even in the hottest region of ECAL. In the Middle ECAL a module is subdivided in 2x2 readout cells having lead as converter, and in the Outer ECAL a module (lead as converter) coincides with a readout cell. The total number of modules is a matrix of 56 columns times 42 rows (see Fig. 1) and the total number of readout channels is about 6000 equally shared among the three ECAL sections. The cells are readout by means of photomultipliers. Signals from photomultipliers are sent into about 40 m long coaxial cables and then fed into the front end driver card (fed). The analog signal is here pole-zero compensated and shaped by means of a 60 ns gated integrator. A 13 bit dynamic range with 12 bit ADC resolution is got by means of a dual slope transfer function with an analog technique based on a fast clamping amplifier [4]. The 12 bit digitized data are stored into DPRAM 256 cells deep for the data acquisition (daq) second level buffer. This early digitization is an important feature for the HERA-B ECAL pretrigger system, since it allows, after a data conversion made by lut in the fed card [3], to obtain absolutely energy calibrated data and to perform digital processing of the data themselves in order to extract all the relevant quantities for the electron trigger algorithm. An important feature implemented on the readout board is the availability of a fast (< 100 ns shaping time) analog sum over its 32 channels. Starting from this signal a fast inhibit system based on the rejection of events with too large a deposit of energy in the Inner ECAL has been designed.

2.2 The HERA-B electron trigger strategy

Electromagnetic cluster in ECAL are looked for in a 3x3 matrix of readout cells. For each readout cell an energy threshold $E_{th}$ function of the cell coordinates is defined as $E_{th} = K_{trig} \cdot \left( \frac{1}{\sqrt{x^2 + y^2}} + \frac{1}{\sqrt{x^2 + z^2}} \right)$, where $x$ and $y$ are the center of cell coordinates and $K_{trig} (GeV/cm)$ is an adjustable parameter. This threshold
Fig. 1. The HERA-B ECAL partition in shashlik type modules. In this picture it is also shown the partition (dashed lines) in pretrigger boards (one processor per board). The partition is in 8x6 readout channels matrix for the Middle and Outer ECAL, and in 10x5 readout channels matrix for the Inner (two close modules in the horizontal direction). This latter is not highlighted by dashed lines for sake of picture clarity.

function actually apply a transverse momentum cut keeping into account the non uniform particle distribution due to the bending of the magnetic field. The algorithm adopted to individuate an electromagnetic cluster (candidate) is the following (refer to Fig. 2):

- 1) $E_5 > \frac{E_{th}}{2}$
- 2) $E_5 = \max(E_1,...,E_n)$
- 3) $\sum_{i=1}^{n} E_i = E_{TOT} > E_{th}$
If a candidate satisfying conditions from 1 to 3 it is found, the pretrigger should calculate also the following quantities to form the messages to be passed to a ROI in the tracking system:

- center of gravity of the electromagnetic cluster corrected for the non uniformity of response of the calorimeter cell;
- address of the ROI;
- a flag which indicates whether the electromagnetic cluster transverse momentum is above a preset threshold (to trigger on high $p_t$ photon candidates);
- the energy loss by the electromagnetic cluster for bremsstrahlung (BS) photon radiation (if any).

The guidelines to face these tasks and underlying the HERA-B electron pretrigger design are the following:

- follow the general HERA-B experiment FLT criteria: minimize number of processors by moving the processes to the stored events data rather than all the data to distributed processing units
- keep flexible the processing unit calculation capability, using LUT based processors.

These criteria have been fulfilled by the following hardware implementation of the required algorithm:

- i) apply condition 1 at the very early stage of the data readout (in the FED boards);
- ii) apply a fast local energy maxima algorithm (condition 2) at the very early stage of the pretrigger board.

Step i) gives a strong reduction on the possible electromagnetic clusters to be processed; step ii) is fundamental to address the central cell of a cluster as well
as the eight neighbour cells, and to pass the nine energy values and central
cell coordinates to the data processing unit that evaluates all the parameters
relevant for the FLT. In the global design of the pretrigger system the three
different ECAL regions are treated as independent; Monte Carlo simulations
have shown that this simplification worsens the overall electron pretrigger
efficiency for the $B^0 \rightarrow J/ψ K_S^0$ channel by a 2%. A system of patch panels
from the front end boards fans out the signals belonging to the borders of
regions covered by close pretrigger boards (see ECAL partition in pretrigger
boards in Fig; 1). In this way there is no loss of efficiency due to pretrigger
cards border effects.

2.3 Technical description

On the readout board the ADC output 12 bit data is fed into a 4kbyte LUT
that gives as an output a 8 bit word in which 7 bit represent an absolutely
calibrated energy datum compressed following a $\sqrt{E}$ law (the error on the
energy resulting thereby constant all over the energy range). The 8th bit is a
flag containing the information whether the energy of the readout calorime-
ter cell fulfills the condition 1 of the electron pretrigger algorithm (since the
constant term for the calorimeter tower energy resolution is at level of 1%, it
makes no sense to use more than a 7 bit information for the calculation that
can be performed at pretrigger level). This 8 bit data is sent to the pretrigger
card according to a serial synchronous protocol. Two groups of 4 bit each are
transmitted by means of two wires at a clock frequency of 4 times the one of
the HERA-B clock (running at 10.4 MHz). In Fig. 3 a block diagram of the
HERA-B ECAL pretrigger card is shown. A pretrigger card can process the
data from a 10x5 (or 8x6) matrix of central cells and 34 (or 32) border cells
(see Fig. 1). The logic blocks shown in Fig. 3 perform the following operations:

- **Input Interface (IIF):** it accepts the 8 bit serial data, converts it into
  parallel and stores it into a DPRAM 64 events deep.

- **Local Maxima Finder Unit (LMFU):** It is the most important block to
  perform the clustering algorithm: 8 bit serial data from each of the 50 (48)
  input channels are processed in a serial way, condition 2 (see Section 2.2)
  is checked only for the data that have passed condition 1 (8th bit issued),
  and the coordinates of the local energy maxima are found. The algorithm
  performed by this unit represents an original feature of the pretrigger board
  design and it is described in detail in Ref. [5].

- **Process Controller (PC):** it performs a 16 events deep three-fold pipelin-
ing of the addresses of the candidates found by the Local Maxima Finder
  Unit and a 16 events deep four-fold pipelining of the addresses found by
  the Bremmsstrahlung Request Interface (see below). A priority logic decides
which one of the seven pipelines has to be depleted at each clock cycle according to an algorithm described in Ref. [6]. This algorithm allows to process up to 3 candidates per board which is well beyond the rate of electron candidates per BX expected in HERA-B (2 per BX all over ECAL).
- **Event Buffer and Multiplexer (EBM):** it allows to extract, starting from the central cell address given by the Local Maxima Finder Unit, the 7 bit energy values of the central cell itself and of the eight neighbour cells.

- **LUT (Data Processing Unit, DPU):** it is the data processor. It is implemented in LUTs (see Fig. 5) that perform all the computation needed to form the electron pretrigger message starting from the 9 (3x3) cluster energy values sent by the Event Buffer and Multiplexer and the cluster central cell coordinates. This unit is flexible as far as concerns the pretrigger algorithm choice and possible updating of it. The DPU processing time to extract all the parameters relevant to the FLT is 1.25 HERA-B clock cycles (about 125 ns).

- **Bremsstrahlung Request Interface (BRI):** It represents another original and important feature of the design of the electron pretrigger for the HERA-B experiment. Due to the presence of material between the interaction point and ECAL, the electrons/positrons may undergo radiative energy loss by means of BS radiation. If the loss of energy happens before the magnet, the distance between the electron/positron and the photon impact points on ECAL are fixed by the kinematics. The algorithm implemented in the HERA-B electron pretrigger boards (in order to associate the possible photon energy to the main electron/positron candidate) is the following (see Fig. 4):
  · starting from the total electron/positron energy evaluated in the DPU the ECAL coordinates where the possible BS photon energy has to be searched are calculated;
  · these coordinates are sent to the BRI which issues a request either to the PC inside the board itself or to the two PCs of two (due to the electron/positron ambiguity) external boards (by means of J3a/J3c connectors in the VME bus);
  · the PC addresses the EBM and the total energy (on a 3x3 matrix) of the BS photon is evaluated by the DPU; if the evaluated datum belongs to an external board with respect to the requesting one, it is sent back via J3b to this latter board;
  · when this cycle of operations has been accomplished, the final message is composed in the FIFO on the board with the electron/positron candidate; besides the candidate energy, the message to be delivered to the TFUs contains at this point also the two possible values of the BS photon energy.

- **VME interface and Message Formatter (MF):** An 80 bit message is formed here containing all the quantities elaborated by the DPU and necessary to the FLT track finding unit (TFU) processors to elaborate the trigger algorithm. These messages are then sent to the TFU Interface (TFUI) that transmits them in four 20 bit packets at a clock frequency of 100 MHz. A prompt logic signal is also formed in this unit when an electron candidate satisfying all the algorithm requirements has been found. This output allows to trigger ECAL also in standalone mode without TFUs for
Fig. 4. The bremsstrahlung recovery algorithm flow diagram. Processes performed in the board of the electron/positron candidate are in the elliptic blobs, while processes performed on boards external to the candidate one are in the rectangular blobs.

deeding purposes, or to give a further condition to the FLT concerning the total number of candidates in the whole electromagnetic calorimeter per event.

- **FCS Interface (FCSI)**: it is the interface, common to all the subdetectors, to the clock of the experiment. A 7 bit BX number is delivered to this interface that is used for data addressing and labelling.

The electron trigger system works synchronously with the BX up to the Message Formatter stage, while the transmission of data to the FLT TFU is as well as the remaining logic of the FLT are asynchronous.

The whole pretrigger logic is implemented in 4000 Series XILINX FPGAs. All the logic operations inside the board are performed with a clock running at about 40 MHz (4 times the HERA-B clock frequency).

The total latency to process one candidate (without taking into account the BS recovery operation) is 15 HERA-B clock cycles (about 1.5 μs).

Prototype versions of readout and pretrigger boards have already been tested on bench and on beam. The interfacing of the pretrigger card to the readout board and to a prototype version of a TFU board has also been tested suc-
The pretrigger active (exploiting some of its functions) is being intensively tested.

In the picture refers to different computational blocks.

Fig. 2. The HERA-B ecal pretrigger data processing unit. The different blocks are connected.
The experimental situation in which the LHC-B electromagnetic calorimeter will operate, under many fundamental respects, is similar to the HERA-B one. Also in this case an electromagnetic cluster ID has to be performed in a situation in which there is a considerable number of channels with only few candidates per event. For this reason the adaptation of the HERA-B electron trigger scheme to LHC-B is in principle feasible. The critical, but technically affordable, points concern of course the input and output stages of the pretrigger card: the former (up to the LMFU output) since it has been designed in order to accept data at the HERA-B clock frequency of 10.4 MHz; the latter since it has to be interfaced to logic unit that in principle could differ from the TFUs. Anyway it has to be stressed again that the present version of the pretrigger cards works at about 40 MHz, i.e. the same as the LHC-B clock frequency. Once the incoming data have been reduced by the LMFU, the adaptation of the two schemes is mainly a matter of proper dimensioning of the intermediate stage processing pipelines. From this point of view it has to be considered that, even if the LHC-B clock frequency is 4 times the HERA-B one, the number of candidates per unit of time to be processed by the two experiments is expected to be comparable [9]).

The data transmission to the readout and the pretrigger card is not expected to represent a problem. Commercially available serial links may guarantee a proper data interfacing and moreover may bring to a reduction of the cable interconnection number.

The problem to be considered from the technical point of view is the increase by a factor of four of the processing capability of the LMFUs. Solutions to overcome this problem can be found also with today available techniques (i.e. ASIC implementation of the LMFU). One could for instance consider a number of LMFU (less than 4) working in parallel, this number depending on the maximum clock frequency at which the ASIC version can work.

An ASIC implementation of the major logic components of this scheme could lead also to a better integration of the system and finally to an increased number of channel handled by one board.

### 3.1 Electron and hadron L0 trigger algorithms for LHC-B

The LHC-B electron (and hadron) L0 trigger algorithms, proposed until now, look at first more demanding than the HERA-B ones since that they involve the processing of data from other detectors besides ECAL (HCAL,preshower, pad chamber).

In Table 1 a comparison between the HERA-B pretrigger and the LHC-B L0 electron and hadron algorithms (as derived from Refs. [7],[8] is performed).
Table 1
Comparison between LHC-B L0 and HERA-B pretrigger algorithms. $E_{HCAL}$ and $E_{PS}$ are respectively the energy release on HCAL and the LHC-B preshower. $E_{MIP}$ is the energy released by a minimum ionizing particle in the LHC-B preshower. The other symbols have been defined in the text.

<table>
<thead>
<tr>
<th>Algorithm</th>
<th>LHC-B</th>
<th>HERA-B</th>
</tr>
</thead>
<tbody>
<tr>
<td>3x3 Clusters</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>$E_S &gt; \frac{E_{th}}{2}$</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>$ETOT &gt; E_{th}$</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>$E_{HCAL} &lt; 0.1\ ETOT$</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>$E_{PS} &gt; 3\ E_{MIP}$</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Center of Gravity</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Extrapolate to chamber</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Bremsstrahlung Recovery</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

One thing to be noticed is that the LUT based DPU of the HERA-B pretrigger allows a good flexibility in the choice of the algorithms and it will be shown in the following how it can fulfill the LHC-B L0 electron and hadron needs.

Another problem to be faced in the hardware implementation of the LHC-B ECAL and HCAL L0 trigger is the matching granularity between the two detectors:

do the present status of the detector design foresees that four ECAL towers match one HCAL tower (4:1 option). This solution has been preferred, after simulations, to the original one in which one ECAL tower matches one HCAL tower (1:1 option). For the sake of generality in the following we will show possible hardware implementations for both (1:1 and 4:1) options.

A possible implementation of a joint ECAL and HCAL L0 trigger by means of the HERA-B electron pretrigger logic and under the hypothesis of ECAL and HCAL matching granularity could be carried out as follows:

- a) identifying from the very early readout stage the kind of cluster using a joint information from preshower, ECAL and HCAL. This could be done, like in the HERA-B first step trigger algorithm, by applying energy cuts on the single cell energy release of ECAL and HCAL;
- b) sending to the pretrigger board the total (ECAL+HCAL) energy of the single cell with a two bit flag identifying if the event is a candidate for the L0 trigger and if it is a hadron or an em cluster;
- c) processing the events with the logic unit described for the HERA-B pretrigger board. Depending on the em/hadron flag different algorithms and cuts may be performed by the DPU;
- d) outputting a message containing, besides all the relevant parameters (e.g.
Fig. 6. A possible readout scheme for the hardware implementation of a joint ECAL plus HCAL L0 trigger for LHC-B using HERA-B electron pretrigger processing unit

the total shower momentum, the shower center of gravity coordinates) necessary for the next L0 trigger calculation, also the address of a ROI in the pad chamber.

For further step processing (search for a hit in the addressed ROI and final L0 trigger decision) a logic unit derived by a simplified version of the HERA-B TFU [1] could be proposed (see Section 3.2). On this basis one can estimate a total ECAL and HCAL L0 trigger latency less than 2 µs.

Step a) could be implemented using the front end electronics shown in Fig. 6. In this scheme only the logic components relevant for trigger purposes are considered 1. The analog signals from the three different detectors are shaped and converted to digital. In this scheme the converted signal from the preshower is sent to a lut-ps unit where it is compared with the energy release in the ECAL readout channel. The converted signals from ECAL and HCAL are fed into respective LUTs (lut-em and lut-h) which output an absolutely calibrated energy datum compressed following for instance a $\sqrt{E}$ law. The lut-ps, lut-em and lut-h outputs are fed into a further LUT-EH in which data are processed depending on the status of the LUT-ps output bit and the ECAL and HCAL energy values. The LUT-EH output contains the total single cell energy and two bits identifying the kind of cluster and ; this datum is then serialized and fed into one channel of an L0 trigger processing unit (the HERA-B electron trigger card).

The scheme described has many noteworthy features:

- it is general; also in the case of a non matching granularity between the two calorimeters (4:1 option), the scheme can be easily adapted (see Fig. 7) at the expense of increasing the number of L0 trigger processing units;
- it is flexible on the algorithms: the use of look-up tables allows to perform the hadron/electron discrimination using all the information available at the very first stage; algorithms based on a comparison between the ECAL and

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1 The circuit elements notation reported from Fig. 6 to Fig.11 will be referred to with a bold font in the text following.
preshower energy releases could be simplified by substituting the \texttt{lut-ps} of Fig. 6 with a programmable comparator and disregarding the comparison between preshower and ECAL energy release in the corresponding channel; it minimizes the number of L0 trigger channels: ECAL and HCAL channels can be treated by the same processing unit (this is not true in the case of option 4:1 (see Fig. 7);

The scheme presented in Fig. 7 is a direct consequence of the one in Fig. 6: here the option 4:1 imposes to consider groups of four preshower channels, 4 ECAL readout channels and one HCAL readout channel. Each \texttt{LUT-E} unit handles, besides its own ECAL readout channel energy, signals from the corresponding preshower channel, and from the HCAL readout channel that overlaps the ECAL one. The four \texttt{LUT-E} outputs shown in Fig. 6 are sent to 4 independent channels of a L0 trigger electron processing unit via a serial link. The \texttt{LUT-H} unit handles, besides its own HCAL readout channel energy, the signals from the logic or (or some other logic combination) of the 4 preshower readout channels corresponding to the HCAL one, and from the total energy sum of the corresponding 4 ECAL readout channels. The \texttt{LUT-H} output is then fed into one channel of a L0 trigger hadron processing unit via a serial link.

The number of L0 trigger processing units increases of 25%, but in principle the option 4:1 can be managed by this scheme.

One of the limitation of the two schemes proposed is that they use the 3x3 matrix information not from the beginning of the processing and that they mix ECAL+HCAL information at the very early stage of energy data conversion.
Fig. 8. The most general hardware implementation for the ECAL and HCAL L0 trigger using HERA-B electron pretrigger processing units. It is based on the bremsstrahlung recovery capability featured by the HERA-B boards.

This limitation could be overcome by the scheme proposed in Fig. 8. It is a very general scheme for the implementation of the LHC-B ECAL and HCAL L0 trigger and it is based on the BS recovery option featured by the HERA-B electron pretrigger boards (see Section 2.3).

The guiding idea of this scheme is to consider the BS recovery option as an electromagnetic (hadronic) shower energy recovery one. We will describe this scheme under the 4:1 option, but the extension to the 1:1 option is straightforward.

The individual signals from ECAL (HCAL) readout channels are sent to their L0 trigger electron (hadron) processing unit by means of a serial protocol after a processing similar to the one described for Fig. 7; but, differently from the two previous schemes, in this scheme the ECAL and HCAL information are not combined at the readout level. Only the preshower information is used by ECAL and HCAL and no comparison between their signals is performed at this stage. If an electron candidate is found by the L0 trigger electron processing unit, the L0 trigger hadron processing unit is addressed, and the relative hadron energy (if any) is extracted as has been described for the BS recovery in the HERA-B electron pretrigger logic unit (see Section 2.3 and Fig. 4). The final message, relative to an electron candidate, contains also the information about the hadronic reconstructed energy.

With a totally symmetric processing, the final message, relative to a hadron candidate, contains also the information about the electromagnetic reconstructed energy. The ECAL (HCAL) message address a ROI in the pad cham-
Fig. 9. Electromagnetic and hadronic L0 trigger concept for LHC-B developed on the basis of the HERA-B FLT system. The shaded areas on preshower and pad chambers show schematically the ROI addressed by the electron and hadron L0 trigger units.

and this ROI information is added to a message that is finally sent to a L0 trigger decision units. Solutions on hardware implementation for these two latter units (pad chamber signals processing unit and L0 trigger decision unit) can be found taking as a reference other processing units [1] (TFU, Track Parameter Unit, Track Decision Unit) designed for HERA-B (see Section 3.2). The last scheme proposed is quite general since the information about the electron (hadron) energy are kept separate until the last L0 trigger decision stage.

3.2 General hardware implementation for the LHC-B L0 trigger

In this Section we will consider the most general hardware implementation for the LHC-B electron and hadron L0 trigger that can be derived starting from the previous considerations.

The general scheme is shown in Fig. 9 and is a direct consequence of the HERA-B FLT architecture [1].

In this scheme we do not use the information of the preshower at the very early stage of the readout chain (as shown from Fig. 6 to Fig. 7) but in a successive logic step. This gives the maximum flexibility to the L0 trigger algorithm.

The messages generated by the electron and hadron L0 trigger processing units
contain the address to ROIs in the preshower (and in the pad chambers). This address is used to extract pattern of hits in the ROI from a logic unit derived from the HERA-B TFU that will be referred as Hit Finding Unit (HFU). These patterns are processed in order to check if hits are presents in the preshower (and/or pad chambers) addressed ROIs and, if necessary, to refine the electromagnetic (hadronic) shower directions

The HFU output messages contain at this stage all the relevant information to form the L0 trigger for an electromagnetic (hadronic) candidate:

- the hadron shower energy;
- the em shower energy;
- the shower ID of the candidate (em or adronic);
- the preshower flag;
- the pad chambers flag;
- the X and Y coordinates;
- the BX-ID;

These messages are then delivered to a final processing unit, the Trigger Decision Unit (TDU), that performs particle ID (electron, photon, hadron), evaluates the total transverse momentum of the particles, and applies cuts on this quantity.

A block diagram of the HFU is shown in Fig. 10. The preshower (pad chamber) hits are transmitted by means of a serial link and recorded on a DPRAM (HIT RAM, see Fig. 11) using the BX-ID as event identifier. The X and Y coordinates of the candidate are extracted by the L0 trigger electron and hadron processing units message and used, together to the BX-ID, to get the hit maps of the ROIs in the preshower and pad chamber detectors. These two sets of hit maps are processed by LUT-HFU (see Fig. 10) in order to get two separate flags (one for each hit map) and a possible correction to the X and Y original coordinates. The updated message is then sent to a TDU (see Fig. 12) which in a possible version consists of three lookup-tables (LUT-P, LUT-XY and LUT-Pt) that calculate all the relevant parameters for the L0 trigger decision.

It has to be noted that, depending on the final LHC-B L0 trigger algorithm, the TDU's could be implemented into the HFU logic units themselves (thereby reducing the L0 trigger message transmission latency).

In Fig. 10 and 12 are also reported the contribution to the L0 trigger latency of the different logic blocks extrapolated by the HERA-B TFU design (working with a 40 MHz clock). In case the HFU and TDU could be implemented in the same board, the total latency of this processing unit would be 250 ns. The overall latency of the last scheme proposed (Fig. 9) can be estimated, in the worst case (3 candidates per event processed by the same electron (hadron) L0 trigger board), of the order of 3 μs, but there are good reasons to expect that this number be decreased at least a factor of two in the LHC-B time scale; in fact

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Fig. 10. Hit Finding Unit block diagram with latency times (adapted from HERA-B TFU design).

Fig. 11. Hit Memory diagram with latency times (adapted from HERA-B Wire Memory design). In this picture only the part corresponding to one of the two detectors (preshower or pad chambers) is shown.

- the em (hadron) shower recovery scheme is more straightforward with respect to the HERA-B BS recovery one;
- the ASIC implementation of the processing units described will allow to work at a clock frequency at least double with respect to the HERA-B present one.
4 Conclusions

The HERA-B and LHC-B early stage trigger needs are similar in many fundamental respects. Due to this fact a rather straightforward hardware implementation for the LHC-B electron and hadron L0 trigger seems to be possible. Some solutions have been described starting from the HERA-B FLT architecture. One of this solutions appears to be very general and quite independent of the final decisions on these items that will be taken.

As a final remark we should like to mention that the experience that HERA-B is gaining on its FLT system could turn out to be a meaningful reference for LHC-B.

5 Acknowledgments

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References

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