LHCb Muon Detector Front End Electronics

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Abstract

General aspects of the Muon Detector front end electronics are presented. Electrical properties of the Cathode Pad Chambers and Multigap Resistive Pad Chambers are discussed and their effect on the choice of electronics is described.
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1 Introduction

The muon detector chambers μ1-5 will provide both muon ID and muon trigger information. The requirement that Level 0 muon trigger be executed in less than 3.2 μs has resulted in the muon chambers being designed with pads in order to make available at the earliest possible moment 2D information about the muon trajectory.

The sizes of the pads in μ stations 1 and 2 are dictated by the the precision with which the trajectory of the muon must be determined in order to give good resolution on muon $p_t$ for the Level 0 trigger and rejection of spurious backgrounds. The sizes in μ3-5 are set by the requirements of clean pattern recognition of penetrating muons. The inner and outer angular coverage of the muon detector based on compromises between available space in the detector hall, economics, sustainable detector rates and balancing trigger rate and $B \to \mu$ acceptance has been determined to be 25 mrad × 15 mrad and 300 mrad x 250 mrad respectively. After studies of pad sizes based on the effect on pattern recognition and Level 0 trigger performance, the pad structure shown in Fig. 1 and given in Table 1 below has has been adopted for μ1.

<table>
<thead>
<tr>
<th>Region</th>
<th>$x$ (cm)</th>
<th>$y$ (cm)</th>
<th>$\theta_x$ (mrad)</th>
<th>$\theta_y$ (mrad)</th>
<th>Pad Size (cm)</th>
<th># of pads</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beam Hole</td>
<td>$x \leq 30$</td>
<td>$y \leq 18$</td>
<td>$\theta_x \leq 24.7$</td>
<td>$\theta_y \leq 14.8$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>I</td>
<td>$x \leq 40$</td>
<td>$y \leq 32$</td>
<td>$\theta_x \leq 34.6$</td>
<td>$\theta_y \leq 26.3$</td>
<td>1.0x2.0</td>
<td>1480</td>
</tr>
<tr>
<td>II</td>
<td>$x \leq 128$</td>
<td>$y \leq 96$</td>
<td>$\theta_x \leq 105.3$</td>
<td>$\theta_y \leq 79.0$</td>
<td>2.0x4.0</td>
<td>5504</td>
</tr>
<tr>
<td>III</td>
<td>$x \leq 240$</td>
<td>$y \leq 176$</td>
<td>$\theta_x \leq 197.5$</td>
<td>$\theta_y \leq 144.9$</td>
<td>4.0x8.0</td>
<td>3744</td>
</tr>
<tr>
<td>IV</td>
<td>$x \leq 368$</td>
<td>$y \leq 304$</td>
<td>$\theta_x \leq 302.9$</td>
<td>$\theta_y \leq 250.2$</td>
<td>8.0x16.0</td>
<td>2176</td>
</tr>
</tbody>
</table>

Table 1: μ1 plane pad structure; each nested inner region is excluded from the next larger region.

The pad structure and sizes of μ2 is the same as for μ1 except the pad sizes are scaled by the $z$ position of μ2 relative to μ1. While the pad sizes in μ3, 4 and 5 are twice as large in the $x$ dimension with respect to the pads of μ1 and μ2 and maintain the same dimensions in $y$ (allowing for $z$ scaling), the same general pad structure is followed. Since the pad sizes are scaled by the $z$ distance from the interaction region, the overall pad structure of the five station system is projective to the interaction region in both the $x$ and $y$ view.

Within a given muon detector station, the muon plane is divided into four transverse regions. The pad sizes increase by a factor of two from region to region proceeding out from the region closest to the beam, thereby keeping the angular coverage of a given pad approximately the same for each region.

With this choice of pad structure, the μ1 and μ2 chambers have 13,000 pads each, and the μ3, 4 and 5 chambers have 6000 pads each, making a total of 45,500 pad channels for the muon detector.
2 Rates in the Muon Detectors

The four muon stations \( \mu_2, 3, 4 \) and 5 buried in the shield operate at relative modest rates with the worst case being the region just above and below the beam in the vertical plane. In contrast, the \( \mu_1 \) station must accommodate rates approaching two orders of magnitude higher. In Fig. 2 is shown the rates/cm\(^2\)/interaction as a function of \( r \), the radius from the beam for the five stations according to a calculation performed using MARS. The 5 KHz per cm\(^2\) level at \( 2 \times 10^{32} \text{cm}^{-2}\text{s}^{-1} \) for an 80 mb total cross section is indicated by the line in Fig. 2. This particle rate is taken at the present time to be the limit at which existing MRPC’s begin to lose efficiency.

3 Muon Detector Electrical Properties

At present, our baseline design uses Cathode Pad Chambers (CPC’s) to implement the \( \mu_1 \) station because of their ability to withstand high rates. The baseline design for stations \( \mu_2-5 \) incorporates a combination of CPC’s in the small angle high rate regions and Multigap Resistive Pad Chambers (MRPC’s) for the bulk of the coverage in the large angle region. The two detectors CPC’s and MRPC’s will have similar cathode electrical properties which are described below. Their timing properties are somewhat different and will be discussed in following subsections.
The large pad sizes in the outer regions of the detector present a large capacitance to any amplifier design and, therefore, generate potential problems for noise and time slewing for those channels. We have chosen to break the largest pads (those in regions 3 and 4) into a set of smaller pads respecting a limit of approximately $\leq 75\text{pf}$ per pad which experience shows is a tractable capacitance. Each sub-pad would have its own amplifier and discriminator with the necessary OR’ing being done locally. In addition, each of the $\mu_{1-5}$ stations is made up either of four (in the case of the CPC’s) or two (in the case of the MRPC’s) detector planes to insure good CPC and MRPC efficiency (and good timing in the case of the CPC’s). The composite signals for each $\mu$ station are formed by either OR’ing or forming 3 of 4 majority logic of the corresponding pads in the various planes at the periphery of each station. The flow of signals from the “physical” pads to the Level 0 pipeline and trigger is shown schematically in Fig. 3.

At the moment our baseline plan is to deploy the amplifier/discriminators around the periphery of the pad planes. Although this choice is not optimal from the point of view of noise performance it would simplify the servicing of the detector.

In the case of the MRPC’s, the pads would be connected to the amplifiers by microstrip transmission lines on the cathode circuit board. The impedance of the microstrips should be $\leq 100\Omega$ in order to limit the pad time constant to $\sim 7\text{ns}$. An implementation of this scheme is shown in Fig. 4. The positioning of the ground plane sets the capacitance of the pads and therefore limits their size (subdivisions). In Fig. 4 the 0.32cm spacing between pads and ground would limit the maximum size to $\sim 50\text{cm}^2$. One could consider using...
lower impedance lines to allow for larger pads, however such microstrips would necessarily be wider and therefore reduce the packing density.

For the CPC’s the baseline plan is somewhat different. The signals will be transported to the periphery of the detector via cables rather than transmission lines. We show in Fig. 5 the cross section of the CPC’s. As can be seen, the placement of the anode wires is asymmetric in the gap between cathode planes. The wires lie closer to the cathode plane which has the pad structure. The connections between the pads and the cables to the preamps is via electrochemically metallized holes from one side of the cathode plane to the pads. The cables are routed in grooves in the honeycomb support structure to the periphery of the detector.

4 Muon Chamber Front-End Electronics

While the hit rate per channel is not expected to be severe ($\leq 50$ kHz) in the muon system, the electronics chain and chamber together must have sufficient time resolution to be able to associate a hit to a specific bunch crossing. The detector signals will be amplified,
discriminated and OR’ed (in case of pad subdivision and station pairs) all locally on the detector. The 45,000 binary signals will be driven to both the trigger and a nearby Encoder and Buffer for storage during the Level 1 formation time. If necessary the driver will incorporate some delay trim to compensate for small variations ≤ 10ns.

4.1 Signal Characteristics

As with any avalanche multiplication device the dynamic range of the signals is expected to be quite large with either CPC’s or MRPC’s (operated in the avalanche mode). A study of a 3 × 3mm MRPC showed a signal range, for the fast electron component, of 10 ∼ 300fC. The time resolution of interest is not the FWHM or σ of a distribution but rather that time interval containing, say, 98% of the hits. For the CPC we estimate Δt_{98} ∼ 20ns [6] and for a narrow gap (0.8mm) MRPC Δt_{98} ∼ 8ns [7].

4.2 Amplifier/Discriminator

In order to terminate the transmission line which conveys the signals from the pads to the periphery of the detector, the amplifier must have a well defined wide-band input impedance of ∼ 100Ω. The capacitance at the input is expected to be large (∼ 150pf); arising from the cumulative capacitances of the pad (75pf) and transmission line (80pf).
This combined with the desired short peaking time suggests [9] the preference of bipolar technology over CMOS for the implementation of the amplifier, due to the lower attainable series noise component with the former. Typical low noise amplifiers made from discrete devices available now have parallel noise \( \sim 1,000e \) and series noise \( \sim 30e/\text{pf} \) at peaking times around 10ns. This would imply a total noise slightly less than 1fC in the situation described above. An example of an integrated bipolar chip incorporating an amplifier and discriminator is the RAL110[8], which was developed for the proposed PSI B-Factory RICH. Since the input is a grounded base configuration it has a broad band constant input impedance as desired. However, its noise performance has not been well characterized in terms of equivalent input charge. Another example of an amplifier/discriminator chip implemented in bipolar technology is the UPENN ASD-8[10]. The input impedance of this design is about 200\( \Omega \) and varies with frequency due to the type of feedback employed.

Assuming leading edge discrimination of the amplifier output the crossing period of the beam sets a limit on the allowable slewing;

\[
\Delta t_{98} + \Delta t_A < 25\text{ns}
\]

where \( \Delta t_A \) is the peaking time of the amplifier with capacitively loaded input. The peaking time \( \Delta t_A \) has contributions from the finite bandwidth of the amplifier and the exponential discharge of the pad \( (RC \sim 7\text{ns}) \). The above timing budget implies a \( \Delta t_A \sim 17\text{ns} \) for the MRPC which allows for about two pad time constants and an intrinsic amplifier rise time of about 5 ns, assuming multiple \( RC \) shaping. The budget with the CPC is somewhat tighter due to the broader \( \Delta t_{98} \), allowing a total \( t_A \) of about only 5ns. The “baseline”
solution to this problem is to derive the timing from an OR of several detectors. Another way to avoid slewing altogether is to use a peak sensing discriminator [11], see Fig. 6. By incorporating sufficient deadtime in the discriminator, spurious pulses due to the extended ionization trail in the 4mm drift region of the CPC should be avoidable.

Figure 6: Peak sense timing to avoid slewing effects.

4.3 Encoder and Buffer

The discriminated signals are sent via LVDS drivers to Encoder and Buffer cards located in crates nearby the detector. The reason to separate the digital functions of the readout from the analog, which is on the detector, is two-fold. First the signals must, in any case, be sent off the detector to participate in the L0 trigger. Furthermore, it is desirable to isolate the 40MHz clock from the potential antenna formed by the pads and connected transmission lines.

The architecture of the encoder and buffer follows that proposed for the generic Front-End in [12]. It is shown in Fig. 7. The modularity is chosen to be 256 channels determined by the desired encoding time under worst case occupancy. The input to a card is 256 binary signals from the detector which are immediately stored in order to allow for L0 formation time. Upon a L0 accept the output of the L0 delay buffer is passed to a small FIFO which smooths the data rate into a 256-to-8 encoder. It is anticipated to have a hardware limit on the number of hits in the 256 channel group in order to limit the encoding time to 320ns (e.g. 32 hits for a 10ns encoding rate). The loss of triggers should be less than 0.33% [12]. After encoding the data is stored in a FIFO awaiting the L1 decision. This FIFO holds the encoded hits and a time stamp for event identification.

At the moment the precise details of this portion of the muon detector readout are incomplete as a large amount of effort can be saved by coordinating the design with that of other detectors having a binary output.

5 Acknowledgements

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References


