A simplified and accurate front-end electronics chain for timing RPCs

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Abstract

Recent advances in electronics and construction techniques have pushed the timing resolution of Resistive Plate Chambers below 50 ps sigma with detection efficiencies close to 99% for MIPs.

In this paper we describe a new front-end electronics chain for accurate time and charge measurement in these devices, having in view a possible application in ALICE’s T0 counter.

The circuit is built solely from commercially available and inexpensive integrated circuits, featuring a reduced number of components. It includes a fast (2 GHz bandwidth) two-stage amplifier that feeds a fixed threshold discriminator followed by an external TDC. The amplified signal is also buffered into an external ADC for charge digitization.

The chain was tested with realistic test signals from an RPC, yielding a timing resolution around 10 ps sigma for signal charges above 100 fC and a charge resolution of 5 fC.
Summary

The recent development of timing Resistive Plate Chambers (RPCs) opened the possibility to build large, high-resolution, TOF arrays at a low cost per channel. Previous work has shown timing accuracies below 50 ps sigma at 99% efficiency for single four-gap chambers [1] and an average timing accuracy of 88 ps sigma at and average efficiency of 97% for a 32 channel system [2].

In this paper we describe a new, streamlined, front-end electronics chain for accurate time and charge measurement in these devices. The circuit will be used in future developments aimed to extend the detector size, to include a position sensitive readout and to achieve better timing resolution and rate capability.

The circuit is made solely from commercially available and inexpensive integrated circuits, featuring a reduced number of components. It includes a fast (2.5 GHz bandwidth) two-stage amplifier that feeds a fixed threshold discriminator followed by an external TDC. The amplified signal is also buffered into an external ADC for charge digitization. A full schematic and PCB layout will be included in the final report.

The test setup included a single-gap RPC as a realistic signal source, feeding in parallel two front-end circuits. The time difference between both timing signals was measured by a TDC constituted by an ORTEC 286 TAC, followed by a shaping amplifier whose output was digitized by a LeCroy 2249B peak-sensing ADC. The amplifier gain was adjusted to give to the TDC a 3 ps bin width and a 6 ns time range. The measured time resolution of the TDC was 3.5 ps sigma. The analogue outputs of both channels were digitized by a LeCroy 2249w charge-sensitive ADC. The fast (electron) component of the signal was selected by a 40 ns gate width. The system was calibrated by an injection of a set of known charges using one of the test inputs, yielding a sensitivity of 3.3 fC per ADC bin, a digitization range of 6 pC and a charge resolution of 5 fC (1.5 bins) sigma.

The timing accuracy of the system was measured by slicing the charge distribution in several regions, applying a linear slewing correction to each slice and doing a gaussian fit to the corrected time distribution of each slice. The results show that the electronic timing accuracy is close to 10 ps for fast signal charges above 100 fC and it is degraded for smaller charges.

Further tests using electronically generated signals injected into single timing channels were performed to compare the present to the previous version of the front-end circuit (used in [1]), based on a pre-amplifier made with discrete components. The results show an evident advantage of the new design for the smaller charges.