"DEAR"

(Digital Event Automatic Recorder)

"Early stage" Description.

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I. GENERAL

1. Purpose of the Instrument

The Automatic Event Recorder is intended to be used in counter experiments for recording counter array pulses produced from a pulsed accelerator (CERN Proton Synchrotron).

By "Event" is meant a certain pattern of pulses obtained during a given time from various sources. The recorder will diminish, by an order of magnitude, the time taken for many complex counter experiments. The instrument is flexible in store and input arrangements in such a way to cope with "unforeseen" experiments.

2. Basic Logical Description

Before entering into the discussion of the simplified diagrams of the instrument (page 16) we would like to point out that due to the possible use of two different output means (see section II.5 Output), the box will offer different possibilities.

Now a paper tape output is foreseen (for economical reasons!) and a magnetic tape output only later, so that figures given are normally for paper tape. If figures for magnetic tape output are different, they will be given in parenthesis. The basic arrangement shows that there are five main logical blocks. A more detailed schematic is given on p.19 and the disposition of the units in the rack on p.20.
a) Principle of operation

If one event - or pattern of several pulses - has to be recorded, a "start of event" pulse is given (see p.19). This signal fires the main gate generator which then triggers all gate generators simultaneously (general case!) or with appropriate delay if necessary (with cables). There are 16 gate generators, each one gating 4(5) inputs. 1 gate generator + 4(5) input circuits is in a plug-in unit. There are 16 plug-in units.

If needed, one of these "pattern" units can be replaced by another type of unit, the "scaling unit". The scaling unit has only 1 input feeding a binary scaler of 4(5) stages. The 4(5) information (counts) is transferred to the ferrite core store in exactly the same way as the 4(5) information of the other plug-in (pattern) where bits are independent. The scaling unit is mainly intended for connection to encoders for pulse-height analysis. See detailed information in section II.2 Inputs.

b) Transfer from "inputs" to "Memory"

Once the pattern has been recorded, and once pulse heights have been converted into counts and fed to the scaling units, the "split gates" or "distribution gates" can write into the cores the information contained in the FF (intermediate memories).

The purpose of these split gates is double: first they must provide the necessary time selection to the cores and in addition they distribute the input signals to the core memory in different ways,
depending on how many inputs are used and how the core memory is connected.

c) Core memory use

\[
\begin{align*}
1 \times 16 \text{ events} & \quad 4 \times 16(20) \text{ inputs} \\
2 \times 16 \text{ events} & \quad 2 \times 16(20) \text{ inputs} \\
4 \times 16 \text{ events} & \quad 1 \times 16(20) \text{ inputs}
\end{align*}
\]

All these figures are maximum values and smaller values can be used.

d) Adjustment of maximum event numbers

\[
\begin{array}{lll}
\text{Case (i)} & 16 \text{ events maximum} & \text{possible adjustment} \\
\text{Case (ii)} & 32 \text{ events maximum} & 2,4,6,16 \text{ events} \\
\text{Case (iii)} & 64 \text{ events maximum} & 4,8,12,32 \text{ events} \\
\end{array}
\]

e) Intervals during main gate signals

This is the time elapsing between each "write-in" period (one pattern). The shortest time is given by the core circuitry and logic. Since there was no precise or hot requirements, we choose
13 μsec as an approximate minimum. The main gate generator is, of course, dead during this time so that other main gate signals occurring remain without action.

This dead-time period can be made longer if necessary - due to pulse-height decoding time. Maximum adjustment dead-time will be 1 ms, then \( \infty \), this last value meaning that an external reset or "END of EVENT" must be provided before next write-in process starts.

f) Read-out

Cores are read out in groups of 4(5) by a timing circuit which is in synchronism with the puncher (or writer). The first model will be equipped with the Teletype Puncher for 110 rows/sec punching. This means that the core store \( 5 \times 16 \times 16 = 1280 \) bits will be read out in \( \frac{1280}{4.110} \approx 2.9 \) sec. Of course, some spacing is needed and some labelling of the burst number, so that one gets the following tape arrangements:

For more details see detailed schematic, p. 19 - "Output tape".
The spaces are made to allow cuts in the paper later. STOP and START are necessary signs for the computer, the STOP being a check signal for the number of rows (Nr) being written. Nr must be given to the programme later. Burst number is a number corresponding to a scaler. This scaler is driven by each burst of the accelerator or each read-out (see switch position) and allows the physicist to make any correlation between a possible change of experiment parameters and this number in his notebook and later on in the programme.

The possibility of writing letters directly or parameters in a flexible way on the tape with a typewriter or teletype was studied. The decision to simplify as we did was taken to avoid any error that could be typed on the -very often - night experiment! So in the case of change of parameters or special observations, the following must be done: look on burst scaler, note this number in correlation with new parameters or observations. The programme - on a separate tape - will be done later, and then make use of the noted information. The two rows called "labelling" are to be considered more as a reserve for repetitive change of some parameters during experiment (example: + or -).

g) **Choice of read-out system**

It is possible for the user to select two main systems:

1) the read-out of the memory after every burst of the accelerator (a synchro signal must, of course, be provided);

2) the read-out is made when the memory is "full". "Full" means that the number of events E that was selected before hand is attained. Read-out is then made without considering machine burst.
h) Punch time

As already seen, the time to punch space, start, scaler, labels, core memory, stop and space is approximately 3.1 sec.

We see that for lower energies of the PS a read-out process can be done, say, only every two bursts. The users seem -- for the moment -- to be unconcerned by this limitation. Of course, magnetic tape fully avoids this situation and condenses the total information much more.

II. DESCRIPTION OF THE BLOCKS

1. Inputs

a) Pattern input (or parallel input)

Let us consider one of the 16 plug-in units. See circuit on p. 21. The gate generator produces gate signals of 30 or 100 ns, it can also be always open. The gate signal is common to all 4(5) inputs.

In general this gate generator is triggered by an internally made signal from the main gate generator, in order to avoid getting more than one trigger for one "start of event". This signal is taken from the unit underneath the pattern unit. If one really wants to trigger externally for a special reason, input requirements are as indicated on drawing.

The 4(5) input signals which are matched at 125 Ω must also have characteristics as indicated. The logic of the Event Recorder is
so arranged that the maximum rate of acceptance for input pulses is
approximately 70 kc (13 μs resol.) even if the "start of event" rate
is higher.

b) **Scaling inputs (or serial inputs)**

See circuit p. 22. The plug-in unit is now a binary scaler
with one input (instead of 4(5)) and with a capacity of 16 (32) bits.
Input specifications can be seen on the drawing.

Any pattern plug-in unit can be replaced by a scaling input
plug-in unit or vice versa, only the meaning of the bits is then
different.

Scaling input units can be connected in series for higher
counts.

1 unit → 16 (32) counts $2^4 (2^8)$
2 units → 256 (1024) counts $2^8 (2^{10})$
  etc $2^{12} (2^{15})$

c) **Reset**

It is possible to avoid reset of the scalers between read-out
so that information can be piled up if necessary.

d) **Getting**

Because of its main use in pulse height to pulse number
open encoders, the gate can be always left by means of a switch. In general
a d-c signal coming from the "write-in" logic unit will open the gates at "event start" and close them \(3 \mu s\) after "end of event" (or internally made delayed event start).

2. Split Gates

See circuit p. 23. These are slow gates for connecting input intermediate memories (Flip-Flops) to core Matrix. They are driven by a time pulse and by a "split system" (d-c) corresponding to a certain memory splitting (see section I.2 Basic Logical Description).

The "split memory unit" allows the use of the inputs and the memory in three different ways by opening the necessary split gates at the right time or in the right sequence.

i) 64 (80) inputs (max) 16 events (max)

ii) 32 (40) inputs (may) 32 events (max)

iii) 16 (20) inputs (max) 64 events (max).

By "number of inputs" is meant the maximum number of inputs when pattern units are used only. If scaling units only are used we have then

i) 16 inputs

ii) 8 inputs

iii) 4 inputs

The outputs of the gates are directly driving the half-current amplifiers for the inputs of the core Matrix.
160 gates are needed. For technical, maintenance and spare parts reasons, they were put in three identical units, each one containing 60 gates (20 are not used).

3. The Store

See sketch on p. 24. The store was chosen from estimates of the user's needs. It seems that between 80 ≤ 100 inputs were considered as reasonable and something like 10 ≤ 20 events also.

Therefore, taking account of read-out problems (4 tracks for paper to 6 tracks for magnetic tape) the drawn arrangement could fulfill needs with 5 existing standard 16 × 16 matrices in parallel.

The store is a Philips 16 × 16 matrix type B1.668.06.

\[
\begin{align*}
\tau_V & \geq 68 \text{ mV} \\
dV & \leq 21 \text{ mV} \\
\tau_s & = \text{switching time} \approx 2.25 \mu s \\
I_{\text{read or write}} & = 4.05 \text{ mA}.
\end{align*}
\]

A coincidence current system was chosen and since there were two X- and two Y-wires, independent read-write circuits were used.

The requirements for the driving stages are quite different. The write-in address driver must be able to switch maximum 80 cores and minimum 0. This means that the transistor must have a reasonable collector dissipation and provision must be made for having enough volts - sec. Read-out driving stages must be able to switch maximum 5 cores and signal input drives one core only.
To each matrix plane corresponds a track on the tape.

There are 5 read-out wires and 5 output detectors.

4. Output

See p. 25. The output is a power amplifier unit combined with a parity check circuit. Even parity was chosen to get a space code without hole (or magnetic change) when no signal is present. The unit, as all other logical units, was foreseen — as much as possible — as being able to work faster (9 ms for paper tape, 67.2 µsec for magnetic tape).

5. Logic — checks — labels

The logic is divided mainly in

5a) "Write-in unit"
5b) "Read-out unit"
5c) "Cycling unit"
5d) "Memory split unit"
5e) "Step by step operation"
5f) "Checks"

a) Write-In

It gives the necessary timing pulses for the write-in of an event into the intermediate memory and then into the core matrix. This timing is started by a "start of event" coming from outside and only accepted if the event recorder is ready to work.
The event start then produces a main gate signal which is
distributed to the "pattern units" with cables of equal or unequal
length. The gate generators of these "pattern units" trigger and
information is accepted during 30 ns or 100 ns. The "scaling units",
if any, are also receiving their information. The complete pattern
is now stored in the Flip-Flops of the pattern or scaling units.

The "end of event" signal can now start the transfer to
the matrix. Half currents are produced for writing into the matrix
and then address is advanced by one for preparing next pattern
writing.

An "end of write-in" signal goes back into the cycling unit
which determines the next step.

Regarding the "event stop", one should observe two main
cases:

i) event stop is external;
ii) event stop is made internally.

Case (ii) will generally be used because for example in encoders, the
maximum encoding time is known. Case (i) is reserved for special
cases, or if a fixed dead time is to be obtained.

b) "Read-out unit"

It organizes the transfer of the information from the core
store to the paper tape. By means of switches - generally on "normal" -
parts of the output can be suppressed when certain checks are made.
A switch ("step by step") allows the advance of the tape row after row. Each advance being made by the "one step" button.

All the read-out process is synchronized by the puncher. A cable coming from the puncher brings the necessary "synchro". The time sequence of all the information read-outs can be seen on the tape drawn on the block diagram, i.e.:

8 spaces / 1 start signal / Reference scaler /
Parameters / All events / 1 stop signal / 8 spaces.

c) "Cycling Unit"

It provides a link between write-in and read-out, because there are, generally, many (2, 4, ..., 16) write-ins for one read-out.

It also offers the choice for reading out:

i) when memory is full
   (this means when the latest preselected address is reached);

ii) synchronized from an external source
   (example: every burst).

The stop and start operations are also provided in this unit as well as "step by step" operation (see 5e).

The event recorder always stops at the end of a read-out process so that it is ready afterwards to start again. A synchronizing circuit using the first "event start" avoids beginning in the middle of a burst.
d) "Memory Split Unit"

It consists of three sub-programmes giving an output pulse called "memory full" saying that events are filling the memory.

i) "Memory full" for the first time that the last address is reached (E).

ii) "Memory full" for the second time that the last address is reached (E). It is the 32(40) inputs case with 2E events.

iii) "Memory full" for the fourth time that the last address is reached (E). It is the 16(20) inputs case with 4E events.

These three sub-programmes are acting on the distribution (or split) gates, in order to connect the 64(8), or 32(40), or 16(20) to the correct matrix cases, in suitable time sequence.

e) "Step by Step Operations"

The purpose of such facilities is to be able to advance in steps, having time for observations (pattern/pattern or row after row) and for fault finding.

i) One can advance in time "write-in" after "write-in (or pattern after pattern)."

Shift switch from "normal" on "one write-in" in cycling unit. Now the machine will stop after having written in one event. The event can be seen as long as desired on the indicating lamps in the pattern.
or scaling - units. To allow the next write-in push on "Start".

ii) "Normal" \rightarrow "one read-out" then the machine does one read-out and stops. Push on start for continuing.

iii) Splitting the read-out on tape in rows.

In "read-out unit" place switch from "normal" on "step by step", then for advancing output tape row after row push on button "one step".

NOTE: For normal work all switches should be on "normal".

f) "Checks"

The main check consists in the setting of an artificial pattern in the input units ("scaling" and "pattern" units). Each of these 16 units will receive the same 5 bits pattern. This 5 bits check pattern is automatically given and is 1111(1) or 0000(0).

There are two possibilities of giving this artificial pattern:

i) manually by placing switch on "Manual" and then pushing on 1111(1) or 0000(0) pattern;

or

ii) automatically every time that the tens or hundreds of the burst scaler are on 0 or 5 (see "automatic test" on logical circuits).

A two-positions switch on the front panel of "pattern setting" allows the selection of
"Automatic"
"Manual"  > pattern setting

and another one

"Tens"
"Hundreds"

decides if a check is wanted every time the tens or hundreds are on 0 or 5. To obtain a better check the pattern will be 111 ... 1 when on 5 and will be 00 ... 0 when on 0 (Hundreds or tens).

Addresses advance can be suppressed for studying a group of cores which is thought to be wrong. The "full memory" signal is then replaced by a "no advance" signal with the same logical effects.

To stop advance put switch of address ring scaler on "no advance". Any address can be set with the "advance" push button.

Partial output is possible for avoiding paper losses and simplifying checks. One can suppress independently or simultaneously the "labels" read-out, the "store" read-out, the "spaces".

For example, if one wishes to check the "burst scaler" read-out only the "labels" are left in the "normal" position (read-OUT timing unit).

The labels - As we said earlier "labels" consist of 3 parts

1) START and STOP signals; these must tell the computer that now a read-out is beginning and finishing.

These two signs are not fulfilling parity so that the computer can recognize them (as well as the operator!).
ii) Burst scaler - We remember that this is the reference with the historical developments of the experiment.

Please note its content for every variation in the experiment! It may contain one of two values: burst number or read-out number. (Choice with a switch on cycling unit.)

iii) Quick parameters setting

- Can be used for setting special information by means of 8 switches on the "Parameters" unit. Generally (ii) should be used for reference. (iii) is mainly for rapid changes occurring during experiments (+ to -, etc.).

NOTE: Of course the step by step operation (section 5e) is used both for observing the experiment, but mainly also for checking purposes.

III. DISCUSSION

Experience will show the definite requirements for the number of inputs, number of events etc. Experience will also show if magnetic tape is necessary or if another system like punched card must be used. All of the instrument is put in one rack and a carriage with power supplies on which is the paper puncher.
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