QUALITY ASSURANCE AND TESTING BEFORE, DURING, AND AFTER CONSTRUCTION OF SEMICONDUCTOR TRACKING DETECTORS

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Abstract

We discuss the most frequent problems met with during the construction of three generations of microvertex detectors and a silicon-tungsten luminometer for the OPAL experiment, and during the many small projects and R&D work for other experiments and University projects. The emphasis will be on describing technical details and work practices adopted to prevent damage to and loss of expensive material, and the techniques preferred to prevent disaster during construction.

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1 Introduction

During the last few years high-precision silicon tracking detectors have become an essential part of most high-energy physics experiments [1]. In 1990 we set up a facility to construct microvertex detectors for the OPAL experiment [2] at the $e^+e^-$ collider at CERN. It has served to construct and upgrade the microvertex [3], and for the fabrication of the OPAL [4] silicon–tungsten luminometer. Since then, it has served to assemble and bond detectors for other LEP and fixed-target experiments.

Recently a large number of prototype detectors for future experiments at the proton–proton collider LHC have been built and bonded, as well as some detectors for university projects. Those include also GaAs detectors, microstrip and microgap gas chambers.

This report is an attempt to give an account of what we have learned about such detectors, the problems met, and solutions developed to build high-quality detectors with high yield.

2 The building blocks of a silicon detector module

The basic building blocks for the construction of a detector module as discussed in this report are:

a) the detector, a microstrip pad or drift silicon detector or a GaAs microstrip detector. Silicon detectors may have single or double-sided readout. Assembly and bonding of microstrip gas chambers is in many aspects similar to that of silicon detectors, although no attempt will be made to treat chambers explicitly;

b) a multichannel front-end chip with up to 128 multiplexed sample-and-hold readout amplifiers for strip and pad detectors, or multichannel analog amplifier for drift detectors. In some designs a front-end programmable local sequencer is used to control the operations of the front-end amplifier chips;

c) a printed-circuit hybrid carrying the front-end electronics, power distribution, filters for power, and bias voltages or currents, and in some designs coupling capacitor chips for AC read out;

d) a high-resolution printed-circuit fan-in is frequently used to match the pitch of the readout electronics to that of the detector. With pad detectors and two co-ordinate strip detectors the fan-in is used to carry the signals from the pad or second co-ordinate strip to the readout electronics at the end of the module;

e) a mechanical structure including a heat sink on which the components of the detector are mounted (glued).

3 Testing of subcomponents before assembly

Testing of all components before use is a major issue for the successful construction of a detector module. This may appear obvious remembering that a module may consist of many (typically 1 to 10) silicon detectors, up to 20 amplifier chips, a high-resolution multilayer printed-circuit hybrid, and a large high-resolution printed-circuit fan-in. As the assembly of a module progresses, repair and replacement of defective or damaged components becomes increasingly difficult. Ideally every component is tested for full functionality and quality before use. Only components fulfilling all quality criteria should be accepted. Risk of damage is high in all steps of production. After every step of assembly a complete test should be done.
3.1 Testing the detectors

3.1.1 C–V curve

Capacitance versus reverse bias voltage (C–V curve) is a basic characteristic of the silicon crystal. It is not easily measurable on microstrip detectors. Simple diodes of a reasonable size are normally included in the mask design for the purpose of measuring the C–V curve. There may however be significant differences in the measured C–V curve, depending on the detailed structure of the detector and the bias circuit, compared with a simple diode. The charge density in the depleted bulk also varies within the crystal.

3.1.2 I–V curve

The reverse leakage current (I–V curve) is a measure of the minority carrier lifetime or rate of current generation in the depleted bulk. Any defect or damage causing increased leakage current or instability is detected by this test. It should always be measured well above the intended operation voltage. Any increase with time or atmospheric conditions (humidity etc.) is an indication of a problem that might develop with time to prevent proper operation of the detector. The I–V curve has to be measured on the detector itself as any test structure will not help in spotting defects or damage.

3.1.3 Coupling capacitors

If the detector is made with integrated readout coupling capacitors their integrity should be controlled. Depending on type of readout electronics and detectors, defective capacitors may degrade or jeopardize the detector. For designs where the potential difference across the capacitor is small, a simple probe card test (but with a complicated probe card for microstrip detectors) is adequate. Using an automatic bonder, an equivalent quick and cheap test is done by mounting the detector on an insulated support, and connecting a resistance measuring loop between the back plane and the bonder ground. The bond program is modified and run to touch down on the readout bond pads, without applying ultrasound power. Although we now rely on factory tests, we leave this test circuit in place during bonding of detectors in order to monitor any damage done to the coupling capacitors during assembly or bonding.

3.1.4 Bias circuits

Bias-circuit structures as required on AC-coupled microstrip detectors (resistor, punchthrough, FOXFET or resistive channels) are not easily measured on the detector. Separate test structures on the wafer are used to control the value or functionality of these structures.

3.2 Detector readout and control chips

The chips may be controlled for functionality, before dicing, on an automatic probe station. It is important that these tests cover all important parameters required from the chip in operation, e.g. speed, gain, noise, linearity, etc. The readout chips for the microvertex were tested for complete functionality, response, and readout speed before use. In most of our applications the chips went through a final test after dicing, e.g. for the silicon tungsten luminometer 10 000 chips were tested on an automatic probe station after dicing, leaving the chips on a special sticky-film support. The screening was performed using a prototype of the final readout electronics system. The entire set of test data for all channels was stored in a database, that was used to group identical chips for individual hybrids, which in turn were trimmed to obtain uniform response over the entire luminometer for the first-level trigger.
3.3 Fan-in printed circuits

The fan-ins for the second co-ordinate readout are usually large-area high-density printed circuits (the OPAL Z-prints are 60 cm² on 0.2 mm glass). These are made on glass, ceramics, or Kapton. Before any other tests the fan-in metal quality and adhesion should be bond- and pull-tested. Then, after cutting, a full surface visual inspection to spot opens and shorts is done. If the defect rate is acceptably low, shorts are removed by scraping metal bridges with a probe needle and a micro manipulator and cuts are bridged by wedge-bonded wires. High-impedance shorts, presumably due to remnants of the contact metal, are almost invisible and are found by testing with two probes or a special probe card.

3.4 Thick-film hybrids

The most common technique used for making the printed circuit for hybrids is multilayer thick-film gold and glass technology on ceramic (Al₂O₃) or ceramic (BeO) substrates. The metallization is bond- and pull-tested and prints are controlled for shorts and opens. Shorts (pinholes) can normally be removed by electrical discharges while opens are repaired by external soldered or bonded bridges.

4 Assembly of a detector module

Assembly of a module is done in steps. In order to minimize loss of expensive components we aim at doing the most complete tests after each production step.

4.1 Equipping the hybrid

After SMD mounting and cabling, and before gluing the readout and control chips, the printed circuit is cleaned (see Section 6). An electric test of the components and cabling is done. After gluing and bonding the chips, a complete readout and calibration test is done, including control of power consumption and temperature rise, on a dedicated heat sink. Any defective element is replaced, even if there is only one dead or noisy channel. Only defect-free hybrids are used for the assembly of a detector module.

4.2 Assembling a module

The hybrid(s), detector(s), and fan-in(s) are glued sequentially onto the mechanical support structure. Bias bonds are made to the detector(s). The reverse leakage current is remeasured to verify that no damage was done to the detectors during the first assembly. Then the complete bonding of the detectors to the hybrid is done. The order of bonding is chosen such that the bonding from the fan-ins to the amplifier inputs is done last. This allows the monitoring of the integrity of the readout AC coupling capacitors during bonding (see Section 3.1.3).

The completed module is tested and calibrated. Any anomaly is diagnosed and repaired. Bond failures are easily repairable. Defects on fan-ins, shorts or cuts, manifested as anomalous high or low noise on a channel, that were missed at the initial control stage, or were created during assembly, are repaired by bonding bridges or scratching. Readout chips that might have failed are replaced. For one single noisy channel we normally do not take the trouble to replace a chip on the microvertex at this stage in the production. Replacement of damaged detectors has rarely been attempted. It turns out to be difficult to remove a detector without causing damage to other components of the module. On the luminometer project, however, any chip with a single defect channel was replaced. In other non-OPAL projects it is up to the owner to decide what repairs should be attempted.
The microvertex module is stored in a closed support frame allowing connections for external test and calibration, which allows easy handling, testing and storage without risk of damaging the module, provided electrical installation and cabling in the test bench or test beam are correct.

4.3 Damage during assembly

Electrical damage due to electrostatic discharges are avoided by using antistatic packages and having the laboratory equipped with antistatic or conductive floor and table covering. The video screen mounted on the bonder is a dangerous and powerful static-charge generator. It was removed from the machine and installed a metre away.

Mechanical damage is more difficult to avoid. Every newcomer in this game destroys some bits and pieces. Tooling has to be designed and fabricated to make assembly as safe and easy as possible. The cost of an assured vacuum system pays off with the first damaged wafer. Pen-like chip-pickers with a built-in balloon, tend to damage the chip surface because in order to pick up a piece the picker has to be pressed down on the active chip area. They tend to wear, letting the metal tube extend beyond the rubber pad. With the picker connected to a vacuum pump this problem can be avoided.

Silicon or glass pieces left over from dicing are difficult to avoid. If they get caught between the silicon surface and any tool or structure, even a rubber pad, they easily make scratches that damage a detector or electronics chip. Every piece is visually inspected for left-overs from chip dicing. Defective dicing (a very frequent defect) is particularly dangerous as it leaves loose but still attached pieces when the silicon or glass is picked up and put down. A common chip design mistake that aggravates this problem and is also a potential reason for short circuits, is to make dice scribe lines out of metal lines. The metal makes dicing difficult and remains as curled wires on the surface. Significant loss was caused by poorly diced silicon.

The thin glass second co-ordinate fan-in used on the OPAL microvertex is diced by using a diamond glass cutter. The diamond is of selected quality and reserved and used only for that glass cutting. We had some losses due to the diamond’s being used for cutting ceramic substrates. It then left glass splinters along the scribe line of the glass that subsequently landed on the detectors and caused damage. All these splinters tend to get stuck in the soft surface of handling tools and continue to cause damage until they are discovered and removed. In order to minimize losses every tool is scanned for such chips and thoroughly cleaned before use.

Similarly, any surface roughness is sufficient to cause damage if it comes in contact with the silicon. All tooling surfaces that have to come in contact with the silicon must be coated with Teflon or Kapton material.

4.4 Bonding technique

Our experience is limited to ultrasonic wire wedge bonding, using an automatic bonder [5]. The choice of wedge bonding is imposed by the narrow pad pitch on detectors and readout chips.

On silicon detectors the bond pads are always placed over the active area. Even worse are the microstrip detectors where the bonds cover three or more strips. The borders of the diodes are the most vulnerable structure. Vulnerability varies with chip suppliers and wafer runs.

The probability of causing damage is enhanced if the bond wire gets lost and bonding is attempted without wire, something that is difficult to avoid with an automatic
bonder. In order to minimize the risk, we use 17.5 $\mu$m diameter aluminium wire that allows bonding with low bonding parameters, and a flat bond foot wedge. The wedge is controlled by performing a series of bonds without wire on a test detector (we used detectors with low leakage current which were rejected due to long-term reverse current instability). If the leakage current increased by more than 100 nA after 10 double bonds the tool was not used in the production.

In order to use thin wire a significant learning effort and a particular attention to the tuning of the bonder and the choice of bond wedge and accessories are required. The wedge [6] is specially designed to optimize guiding of the wire and minimize risk of damage in case of a lost wire bond operation. The bonder is equipped with a low force spring for 17.5 $\mu$m wire bonding and has a motorized wire despooler to avoid twisting of the wire during the conventional axial pulling of the wire from its 2-inch diameter spool. The wire is a conventional 99% aluminium 1% silicon alloy [7]. Best results are obtained with wire annealed to a breaking force limit of 6.5–7.5 g. A harder wire tends to have too high internal stress and to twist during bonding. With the thin wire we have not attempted to rely on automatic missing wire detection. In order to permit continuous visual monitoring of the process independent of the orientation of the bonder head, a video camera is mounted at right angles with respect to the viewing angle of the microscope.

### 4.5 Gluing practice

The two most common gluing techniques are dispersal of the glue in a thin continuous layer or a pattern of regular dots. We prefer the second method which is simpler. Chips are glued on the hybrids using four or five very small dots of epoxy polymerizing at room temperature or 100 °C. The dot diameter is typically 100 $\mu$m. The chips are pressed down by a soft tool to squeeze the glue and place the chip correctly and flat on the substrate. With this gluing technique the chips can be removed easily if needed, either mechanically or by heating the chip above the transition temperature of the glue.

For detector back-side gluing (N$^+$ implanted and metalled surface) we use any epoxy. For front-side gluing and for double-sided detectors we use silicon glue [8], believed to be particularly clear of alkaline ions [9].

Tooling and glue jigs are designed such that the silicon surfaces never touch a metal or any other hard surface, e.g. ceramics.

The sequence of gluing and the polymerization temperatures are chosen such that the ceramics substrate is never submitted to tear forces. Internal stress in the structure of a module is minimized by using materials with matched TEC wherever possible. The silicon glue however has to be heated to 100°C for polymerization, this is taken into account in the design of the modules and the assembly sequence.

### 5 A few module design criteria

#### 5.1 Hybrids

The hybrid design is made such that all bond pads are on the first (bottom) metal layer. The metal is applied in as thin a layer as possible (typically less than 10 $\mu$m) by silk screening. This layer is processed by photolithography rather than using a serigraphy mask. Particular attention is required to remove the etching chemicals from the porous substrate by immediately baking it at high temperature after processing. Otherwise the chemicals will destroy the adhesion of the metal to the substrate. This technique, although more expensive than conventional serigraphy, results in much better bonding quality and higher productivity since the automatic bonding can be done quickly and reliably.
pad size on hybrid printed circuits should be designed to be as large as is compatible with the pitch and space available. The above-described photolithography technique allows a higher density line structure approaching thin film technology. With conventional serigraphy on ceramic, or conventional gold-plated copper on G10 substrates small bond areas should in general be avoided.

5.2 Thin film metallization

Except for the hybrid printed circuit, all bond surfaces are made with thin film metallization. From the large variety of bits and pieces bonded, the first conclusion is that gold plating always presents surprises. In many cases the reason for problems was understood. Often photoresist or passivation layers were not properly removed. Gold metallization on glass and GaAs detectors is still in the development stage. In some cases the hardness of thin-film gold may influence the bondability adversely. Bonding on gold with aluminium wire requires higher bond parameters than on aluminium, and for gold wire, a wedge with profiled or very rough surface increases the risk of damaging detectors. Bonding at elevated temperature is excluded due to the complicated structure of detector modules.

Bondability on thin-film aluminium pads with aluminium wires is rarely a problem. Excessive oxidation or condensation from the atmosphere may cause problems. Ageing of aluminium is slowed down if it is stored in vacuum or in an inert (non-CO₂) atmosphere. We use cheap freezer boxes, at room temperature, fluxed with argon. In the experiment the detectors are operated in a nitrogen atmosphere (O₂ and humidity less than 1%). Rebonding of these devices is still possible after a few years of operation. Rapid ageing has been observed on glass containing Na, presumably due to diffusion of Na ions through the aluminium.

5.3 Bond pad patterning

The difficult and most common pad pitch for bonding detectors to the readout is 44 to 50 μm. Automatic bonders with large tables are typically designed for 15 μm precision and 5 μm resolution. Bond pad pitch should be as large as possible and standardized, e.g. 48 μm on a readout chip is better than 44 μm. Bonding and programming is easier if the pitch of the pieces to be connected is identical. Pitch adaptors, if used only for that purpose, may be too expensive and increase the number of bonds, and are not recommended if that is their only purpose. Pitch-adaptor patterns on the detectors might be interesting.

The parity of pattern for short and long bonds (double-row bonding) should be standardized. Bond pads should be at least 100 μm long and the rows should be separated by 100 μm. Up to 200 μm, long pads may be useful. A pad width of 40 μm is sufficient on a dense pitch and reduces problems of short circuits. When bonding in a single row and at a pitch of 100 μm or larger the pads should be 60 μm wide. With the above described equipment, bonding at 75 μm pitch is preferable to the bonding in double rows at a larger pitch.

Metal lines between pads on a dense pitch should be avoided wherever possible. Metal lines between pads should be as narrow as possible (less than 10 μm) and preferably passivated with a layer resistant to accidental bonding, which could produce short circuits. Fan-ins are not passivated for several reasons, i.e. cost, yield and repairability. The first pad row should be as close to the border of the chip or detector as possible. Short bonds are easier and faster to do than long ones.
Since we started using 17.5 μm aluminium wires we very rarely make use of spare bond pads, frequently included in the designs, since with the thin wires the bond pads are rarely damaged and rebonding is normally not a problem.

Any piece to be bonded should be designed with an adequate bond test area. A small detector test structure on the wafer is very useful for such tests.

5.4 Engineering

The engineering should take into account all steps in the production and testing. Any structure above the bonding level may become a risky obstacle during bonding. Obstacles up to 5 mm height and close to a bond area (less than 6 mm) can be avoided by setting the rest height in the bonder program sufficiently high, which will, however, slow down the bonding speed. Any higher obstacles need special attention. To be safe, the work piece has to be mounted on the bonder table in such a position that the bond tool is protected by the end stops from reaching the position of those obstacles. Obstacles exceeding 10 mm could interfere with the bond head at any time during bonding. This may complicate the mounting and increase the risk of accidents during bonding, damaging the machine and destroying expensive material. Higher structures may make access for bonding impossible. Height restrictions may vary from machine to machine, although all large table automatic bonders I have seen look very similar.

There may sometimes be good arguments for assembling parts to be connected by bonding at different levels. This significantly complicates the bonding in superposed rows and layers. A level difference of less than 300 μm is strongly preferred in this case. Any complicated geometry should be bond tested at an early stage of the design, using the bonder and tool intended for production. Bonding in a single row is not significantly affected at a level difference of up to 1 mm.

All those problems have occurred on samples designed and mounted outside CERN and brought here for bonding or repair. Sometimes a risky and laborious solution is found, sometimes none.

For large-scale projects, modules and tooling should be designed to minimize handling. Ideally the device should be assembled, bonded, tested and stored on the same and unique support. For OPAL’s microvertex detector several different tools were used for assembly, bonding and testing. These were optimized for each operation. The rate of accidents due to manipulations during mounting and dismounting was however not negligible.

6 Equipment

For the assembly of solid-state detectors an air-conditioned laboratory space with reasonable air filtering is adequate. Expensive clean-room installation is not justified.

Fixed-head (manual) bonders are suitable for small pieces. For large pieces rotating-head automatic bonders offer much more flexibility and adequate productivity for large batches. Typically, an average of 1500 bonds per hour or between 6000 and 10000 per day is obtained. Expensive pattern recognition in the bonding machine is of no use for detector bonding.

We continuously visually control the bonding process since we do not rely on the built-in lost wire detection. We have plans to evaluate some recent bonder models with improved control of the bonding process, to find out how well they are adapted to large-scale detector production in view of future large LHC projects. Some modern bonders
have powerful lost wire detection facilities. Some are not designed to monitor the bonding process continuously.

Expensive pull testers are not needed. For the rare occasions where quantitative pull measurements were required for acceptance testing of new products, a very simple force gauge, as used to calibrate the bonder was used [10]. An experienced operator will rely on manual destructive testing.

A manual probe station with a good microscope on a motorized support and a set of good-quality micro probe holders is extremely useful for diagnostic, testing and debugging. It is also used for removing shorts due to pattern defects or bond accidents [10].

An automatic probe station is almost indispensable for large-scale production for detector and readout chip screening before assembly. We did not acquire one. For the microvertex project, initial screening of the readout chips was performed at Rutherford Appleton Laboratory. The final testing and calibration was done at Queen Mary and Westfield College. The AMPLEX chips used for the luminometer were tested and calibrated on an automatic probe station assembled from four numerically controlled tables (X, Y, Z and phi), available in the lab, a microscope and a special probe card with appropriate interfacing electronics, was mounted on a fixed support.

Dry cleaning of components before bonding is an interesting issue. We are evaluating two methods.

Oxidation in a flow of air at atmospheric pressure exposed to an intense low-pressure mercury quartz lamp light (UV) [11]. The light produces atomic oxygen and ozone which remove organic impurities from the surface. It has been found that this relatively cheap technique can in certain cases improve the bondability significantly. Its usefulness appears to be limited to very thin layers of easily oxidizable materials. SMD mounted line driver and receiver ICs have, however, been damaged if the pigtail connector was not protected by conductive foam. Significant increase in leakage current of a Si detector was observed. By warming the detector to 100 °C it recovered to a level not affecting its operation in an experiment.

Recently a plasma etcher [12] was acquired. It is a powerful instrument to remove selectively different materials. We have used it to remove Photoresist left over on readout chips and microstrip chamber substrates. It also removes polyimide passivation, glue and G10.

Both instruments can, with long enough exposure, produce an unbondable oxide layer on aluminium pads.

Cleaning of the printed circuit of the hybrid after SMD soldering is extremely important for two reasons:

- Any solder flux makes bonding impossible.
- Any trace of chlorine ions will destroy the aluminium wire at the bond foot on the gold by catalysed hydroxylation of the aluminium.

Both defects have occurred. Recently a dedicated multibath liquid cleaner [13] was acquired for the laboratory. The first bath is a hot Zestron [14] bath with ultrasonic excitation and recirculation through mechanical filters. The last rinsing bath is distilled, continuously filtered and demineralized water, with built-in conductivity control. A particular attention is paid to the suspension of the prints in the carrier, i.e. that the hybrids are held vertically and attached cables (pigtails) are hanging downwards, especially in
the drying bath, in order to prevent droplets containing impurities from forming over the bonding area. Since the introduction of this cleaner we have not experienced any problems with cleanliness of hybrids.

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The success of the projects that served as the base for this report is the merit of the concentrated effort by many members of the OPAL Collaboration and technical support group at CERN and in OPAL member institutes.

The close daily contacts between all people working on the projects and their patience in detecting, analysing and solving the innumerable problems met, was the driving force for progress.

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