THE H.P.D. LOGIC

A Digital System for the Transmission of Measurements from Bubble Chamber Photographs directly into a Computer.

by

Tor Lingjaerde

GENEVE
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ABSTRACT

The Hough-Powell Device (H.P.D.) is an apparatus for fast, precise measurement of bubble chamber photographs.

This paper describes the logic and circuitry of the H.P.D., the function of which is to digitize the data, and transfer the coordinates directly into an IBM 709 computer.

In general, the circuitry can be used wherever it is desirable to link a measuring system directly to a computer or, with minor modifications, to a magnetic tape unit.

/..
1. Introduction

A brief description of the CERN flying spot digitizer is given in Ref. 1 and 2. This apparatus which at CERN was known under the name "IEP-X", was renamed "H.P.D." (Hough Powell Device) when on-line operation to the computer was adopted.

This paper is devoted almost exclusively to the electronic parts of the H.P.D., covering the development which has been carried out by Hough and the author at Brookhaven National Laboratory during February 1961 and subsequently at CERN.

Whereas the logic circuitry of the H.P.D. is a result of the co-operation between Hough and the author, the analogue circuitry for generation of the "Track Center" and "Fiducial Pulses" is entirely due to Hough.

2. Brief Description of the System

Attention is drawn to section 6 (Future developments) of Ref. 1 and to the section "Data Processing Systems" of Ref. 2.

Kowarski's proposal to use a separate carrier for the "roads" is still considered to be the best solution. A few rough coordinates per interesting event are taken at the scanning table and punched out on an IBM card together with the data necessary for the IBM 709 computer to identify the picture. (See Fig. 1.)

To measure the picture the procedure then is as follows: the information on the IBM-card is first fed into the computer, which identifies and calls for the correct picture and view. (See Ref. 3).

The computer calculates the "roads" from the rough coordinates, and stores them in its memory. Precise measurements of all bubble images are then transmitted from the flying spot scanner via a buffer memory and the Direct Data Connection* to the 709.

* See section 3.

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The computer now looks for those co-ordinates which fit inside the "reads", stores them, and throws away all the other ones, which are of no interest. This sorting-out process takes place during the scan, and is sufficiently fast to avoid any storage difficulty.

3. **Description of the Operation of the H.P.D. with an On-line 709 Computer.**

   The IBM 709 computer can be fitted with a special feature device which will allow data from non-IBM apparatus to be transmitted directly to the Computer memory. This special feature device is called the Direct Data Connection (D.D.C.) for IBM 709, RPO 80 979, and its function is described in an IBM "Special Systems Features Bulletin" (Ref. 5).

   A brief description will be given here of how the D.D.C. is able to sample information from the H.P.D. and store it in the memory while the computer is calculating according to its main program.

   On Fig. 3, the three blocks to the left belong to the H.P.D., whereas the three right hand ones belong to the IBM Computer. Between the two is a multicore cable, (max. length 70 feet) with 36 lines for input-output information as well as all the lines necessary to synchronize the H.P.D. with the computer.

   The computer, or to be more specific, the D.D.C. can only accept a co-ordinate from the H.P.D. at certain unknown times which depend on the computer cycle time and the program. It is impossible in practice to synchronize the flying spot with the computer because the density of information will vary from one area to another on the picture. A Buffer Memory with a capacity corresponding to the maximum expected number of tracks (including unwanted blobs, dust etc.) per scan-line is connected in between the digitizer and the D.D.C. This smoothes out the information flow. For a given scanning velocity, the maximum average number of tracks which can be measured will of course depend only on the computer-speed, provided the capacity of the Buffer Memory is big enough to take up the information rate occurring on the picture.

...
Here we shall only deal with the case where information is fed from the H.P.D. into the computer. (See also Ref. 3 and 4). For this we need only 18 lines (the least significant ones, pins 18 to 36 on the Receptacle) and four synchronizing signals: "Interrupt", "End of File" (EOF) "Direct Data Demand" (DDD) and "Ready to Read". "Interrupt" and "EOF" are signals transmitted to the computer and are used to indicate to the main program the state of the H.P.D. Here the former corresponds to the initiation of a set of measurements and the latter to their completion. The Ready Read signal indicates to the external device that the computer is ready to receive a coordinate. This is followed by the Direct Data Demand to the computer at the time when the corresponding voltage levels have been set up on the output lines (or Data Buses) of the DDC.

These signals, with the exception of EOF, are drawn (heavy lines) on Fig. 4. In addition several other signals are drawn, which merely describe functions taking place inside the computer itself. (See Ref. 5).

Let us follow the operation of the H.P.D. and the DDC during the measurement of a picture, from beginning to end. First of all the measurement must be prepared, that is the correct picture chosen and the card with the corresponding rough coordinates fed into the computer, together with the program. The program will contain instructions which tell the computer to be ready for an INTERRUPT on the DDC channel (in our case channel B), and also what it has to do when this signal arrives. Once this is done, the motor driving the film stage is started. When the correct (and constant) speed of the stage has been reached, an INTERRUPT will be given automatically.

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The INTERRUPT will do two things: on the H.P.D. side it will ENABLE the Buffer Memory Load-Unload Logic (L-U), and track-coordinates will start pouring into the Buffer Memory. The flying spot has been running all the time. On the computer side the main program will be interrupted after a time, T1, the length of which will depend on what it was doing when the INTERRUPT-pulse arrived.

The computer prepares the data channel to receive the coordinates from the H.P.D., and then turns on the Ready Read Signal to inform the H.P.D. Buffer Memory L-U Logic that it is ready.

It is now up to the H.P.D. logic to decide exactly when a transfer of coordinates should take place. Evidently it does not make sense to unload the Buffer if it is empty. The first condition is therefore that at least one track must have previously been detected. A second condition is that if the Buffer is loading at the instant when the Ready Read Signal occurs, the unloading cannot be started until the loading is complete. A Buffer unload pulse is then automatically given which places a word on the 18 output lines. It remains to inform the DDC that the signals have been established on the Data Buses, and this is the function of the DDD* which is a 7 µs pulse, automatically generated after every Buffer unload cycle. This pulse will immediately cause the data on the 18 cases to enter the DDC-Data Register.

The Data Synchronizer now causes the Ready Read line to fall after a certain delay T2, which might be as long as 12 microseconds, a fact that must be kept in mind when designing the H.P.D. logic.

The final goal is to get our track-coordinate into the computer memory. At the same time as the Ready Read line falls, the computer will know that the Data Register is loaded and will

* For the "read" operation the term "Direct Data Demand" is rather misleading. In fact, it is a strobe pulse.

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allow a transfer to the memory after a Time T4 which depends on the program as well as on how many other channels are connected (and competing) at the same time. (In our case, maximum one other channel). Once the transfer has taken place, the Ready Read signal will be restored, and a new cycle starts.

In this way the coordinates from the picture are transmitted to the computer, until we reach a preset X-coordinate which corresponds to the end of the picture. Here an EOF is given automatically by the H.P.D. logic, and the computer immediately disconnects. At the same time the ACTIVATE line to the L-I logic will fall, inhibiting further transmission to the Buffer Memory.

4. Track Center and Fiducial Pulses

The information extracted from the signal arriving from the Track Photo-multiplier (See Fig. 2 and Fig. 5) will depend on the electronic circuitry treating it. Many ideas exist on how best to do this and only detailed studies of data from actual pictures from different bubble chambers can give an answer to the problem. The group at CERN is at present carrying out measurements of pictures from various chambers. One of the aims is to find out whether the present track circuitry is adequate or not.

The "Track Center" circuitry used at present with the H.P.D. relies on the following principle: (See Fig. 5 and H.P.D. - E - 010).

We define the Track Center (T.C.) to be the vertical line which would divide the area under the pulse and above a certain level into two equal parts.

To find the T.C., the pulse is first integrated. A given time T later this integral is compared with the double integral in a differential amplifier, and a "T.C. step" is produced at the crossing point. The T.C. step is delayed in relation to the time T.C.
by a fixed time $T$, merely resulting in the whole picture including the fiducial marks being displaced.

The track center step is converted into a D.E.C. (Ref. 6) standard pulse at the output of the analogue circuitry to pass on to the digitizing logic.

The output from the Grating Photomultiplier (See Fig. 2) is treated in an analogue circuit (See H.P.D. - E - 009), the main part of which is a differential amplifier into which is fed the grating signal itself and the same signal delayed by half a period. The near sinusoidal signal is converted into a square wave from which again D.E.C. standard pulses are derived, ready to enter the digitizing logic as "Fiducial Pulses".*

5. The Y-Digitizing Process

5.1 Introduction

From the analogue circuitry described in section 4, we receive two trains of pulses:

a) The Track Center pulses (T.C.) which occur a constant time after the flying spot crossed a bubble **.

b) The Fiducial Pulses which are generated as the spot travels across the reference grating.

The pitch of the grating is 25.4 microns. The spot travels at a speed of 4.6 microns per microsecond, yielding a Fiducial Pulse every 5.4 microseconds.

These pulses are counted in the (binary) Y-counter. The counter is cleared at the end of a DARK period (See section 7) and therefore starts at zero at the beginning of each scan-line. The content of the Y-counter indicates the position of the spot at any time. The track co-ordinates are derived simply by reading out

---

* Apart from these two analogue circuits, the system is largely made up from Philips digital blocks and DEC building blocks (see reference 6).

** Provided the bubble was black enough to give a pulse the amplitude of which was higher than a certain preset level, the so-called C-level.
the Y-counter every time a T.C. pulse occurs. Special precaution must of course be taken to inhibit read out when the counter is counting.

The grating signal, and therefore the Fiducial Pulses, is accurate to \( \pm 3 \) microns, so it is meaningful to interpolate between them. The interpolation is made in the digitizing part of the circuitry.

5.2 The Basic Principle

The digitizing process will be described in detail, referring to the basic block-diagram BS4 (Fig. 6) and the oscillograms on Fig. 7.

Assume that a Track Center pulse arrives at a time \( T \) during the LIGHT period and sets the Track Center Flip-Flop. The Interpolation Pulse Generator (I) is thereby released and will start to generate interpolation counts at a frequency corresponding to 16 counts per Fiducial Pulse period. These pulses are counted by the Interpolation Counter. The next Fiducial Pulse arriving will reset the T.C. Flip-Flop and stop the Interpolation Pulse Generator. The interpolated co-ordinate of the track can now be found by taking the number contained in the Y-counter (Y5 to Y15) just before the T.C. pulse arrived and adding the complement of the I-counter to this figure*. The actual read out takes place 1 \( \mu \)s after the Interpolation Pulse Generator was stopped, that is just after the last Y-count.

The method described above ensures that the transfer of the co-ordinate (through the AND-gates) to the register can never take place when we are counting. The one bit too many in the Y-counter merely shifts the whole picture including the fiducial marks to one side, and is therefore not important. The complementing of the I's is of course done by reading out the '0' outputs of the I-counter Flip-Flops.

* Example: (in decimal). If the Y-counter contained 64 and the I-counter 4, the track co-ordinate is 64 \( 12/16 \).
At the end of this process we have got a binary coded track co-ordinate in the XY-register. We must not keep it there longer than strictly necessary because there might be another Track Center Pulse arriving. We know that a transfer can only take place 1 μs after a Fiducial Pulse. One feature of the H.P.D. - T.C. Pulse Generator is, however, that two tracks as closely spaced as 25.4 microns (on the film measured between the track centers) will not be distinguished as separate. Therefore at least 10.8 microseconds will elapse before the XY-register is needed again and within this time the coordinate has been transferred into the Buffer Memory. How this is done will be described later.

5.3 The Circuit Diagram

As the difference between Fig. 6 and Y-COORDINATE SECTION on the Logic Master Diagram (H.P.D. - E - 001) is rather small, we shall immediately proceed to the detailed schematics "Y-co-ordinate Digitizing Logic" (H.P.D. - E - 002) and "XY-Counter and XY-Register" (H.P.D. - E - 004). In addition, the oscillograms on Fig. 7 should be consulted during the explanation that follows.

The "Track Center Step" generated in the analogue section will generate a negative DEC fast pulse at A3J. This pulse will be referred to as the TRACK CENTER PULSE (T.C.). Provided that the "AND" gate A1lX is enabled*, the TRACK CENTER FLIP FLOP on Diagram H.P.D. - E - 002 will be set and thus release the INTERPOLATION CLOCK (A12) which will start to oscillate, the first pulse arriving after 0.34 μs. Following the path of the Interpolation pulses, we turn over to H.P.D. - E - 004 where they are seen to enter first stage of the I-COUNTER at B12Y.

* The so called BLOB INHIBIT signal arriving from the Analogue Section will inhibit the digitizing process if the detected spot on the film is much larger than a normal track-width.
The I-CLOCK will continue to run until the T.C. flip-flop is reset by the first FIDUCIAL PULSE that arrives, that is after a maximum of 5,4 μs. The CLOCK has been set to a frequency that will produce 16 Interpolation pulses for one Fiducial Pulse Period. If the I-Counter reaches the binary number 1111, the "AND"-gate B11 will inhibit the input gate B12X, and the counter is blocked. This is a safety precaution which will prevent the I-Counter from "turning" to a second cycle, thus creating an error corresponding to a Fiducial Pulse period.

We now return to the Track Center flip-flop to see what happens when it is reset by the next FIDUCIAL PULSE arriving. The negative going level-change at AllF will produce a fast DEC pulse at A3M which immediately stops the I-CLOCK. The actual track digitizing is now done by transferring the content of the I- and Y-counters into the XY-register before the next FIDUCIAL PULSE arrives, that is within 5,4 μs. The transfer is executed by strobing the AND-gates AI (position B10 on H.P.D. - E - 004) and AY (position B17 and B18) with a negative DEC slow pulse, which is generated by the Pulse Amplifier A16E. But before strobing we must be sure that the Y-counter has settled, and therefore there is a delay of 1 μs (A17) between the END OF INTERPOLATION and the AY-STROBE.

The AY-STROBE will also transmit a load demand to the Load Unload-Logic, and the transfer from the XY-register to the Buffer Memory will be executed within a maximum of 8,5 microseconds as explained in section 7.

Once the transfer to the XY-register has taken place (i.e. after every "Track Digitizing Process"), the I-counter is cleared by a DEC fast pulse which is delayed 0,6 μs relative to the AY-Strobe (A16 and A15E).

* It should be kept well in mind that the I and Y-counters are separate and independent.
When the TRACK CENTER flip-flop was set, it also triggered a single shot (A9), the result of which was that the input gate A3U was inhibited for 7 μs. This is to make sure that a second T.C. pulse cannot arrive before the digitizing process has been completed and the I-counter reset.

The mixing of the 5 μs inhibit pulse (A9J) with its delayed pulse in the "OR" gate A8L is merely done to allow A9 to recover before a new T.C. pulse arrives*.

5.4. The Fiducial Pulse Control and the Dark Signal.

The number of FIDUCIAL PULSES per sweep is given by the number of lines on the reference grating, and is therefore constant. It is desirable to check this number at the end of each sweep, and this can conveniently be done by the computer.

The flying spot generator has been constructed so as to give a DARK-PERIOD of 1 ms between two successive LIGHT-PERIODES.

At the end of the sweep, that is at the end of the LIGHT-PERIOD, which lasts for 6.5 ms, a DARK PULSE as well as a DARK LEVEL is generated by the (modified) delay A10**. As shown on the oscillograms Fig. 7, the DARK PULSE arrives after the last FIDUCIAL PULSE, and after 1 μs, it strobes the AY AND-gates, as shown on H.F.D. - E - 002. From then on the transfer to the Buffer Memory is carried out as described under point 5-3.

5.5 The Y-Counter Reset.

We recall that the INTERPOLATION COUNTER is cleared after each AY-STROBE, that is as many times per sweep as there are (accepted) tracks plus one for the total grating count.

* See also Appendix 4.
** The modifications are merely the added components shown on H.F.D. - E - 002.

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The Y-COUNTER is cleared at the end of each scan line. This is done by gating the DARK LEVEL with the CLEAR-I pulse in the "AND" gate A15X, transforming the DEC fast pulse into a DEC slow pulse by means of the Pulse Amplifier (with feedback) A18M and triggering the 10 µs single shot A21 shown on schematic H.P.D. - E - 004. We know that the CLEAR-I pulse does arrive at the right instant because of the "Total Grating Count"-strobe.

The pulse that clears the Y-counter must have a duration that is longer than the transfer time through the total counter, that is a few microseconds. The reason why it is set to 13.4 µs (the 10 µs indicated on H.P.D. - E - 004 is the minimum value) is that the Y-CLEAR-END pulse is used to initiate the process that transfers the X-coordinates into the Memory each DARK period (See Fig. XI: H.P.D. - E - 012). This is explained in section 6.

6. The Buffer Memory

Several firms are today able to deliver Ferrite core memories with built-in read-write logic. A general purpose memory (Type RBA) from Telemeter Magnetics, Inc. (Ampex) was chosen. The capacity is 128 words each of 18 bits, and it operates in the interlaced, sequential load-unload mode (BQ-operation).

A detailed description is given in the T.M. Manual, but a short abstract will be given here for the sake of convenience.

Seen as a "black box" the memory has, apart from the 18 data buses, only two other input lines which are important in our case: one for a LOAD-command and one for an UNLOAD-command. To load a word into the memory, the particular word is presented as DC levels on the data bus (0V for '0' and 6V for '1').

At the same time a SYNC.-PULSE (0.8 µs long) is given on the LOAD input by the external Load-Unload logic. This pulse transfers (strokes) the presented word into the internal Memory Register. The memory then has to be left to itself for 5 µs. During this time it finds the correct address of where to store in the magnetic module, by adding 1 to the last address where it loaded, and stores the word there. Then, after 5 µs, it is ready to load or unload again.
When a stored word is wanted on the output lines, in our case when the Ready Read line comes up, the external Load-Unload logic gives a sync.-pulse on the UNLOAD line. The memory logic looks up the last unload address in the internal Address Register, adds 1 and after 5 µs establishes the word contained in the magnetic module with this address as a DC signal on the output lines where it remains until a new unload or load command is given.

Example: Assume that the memory is first cleared by a "Master Clear Pulse". We then load say 10 times in sequence, unload 3 times and finally load once. The memory will proceed as follows:

1: Load at address 1, 2, 3 ----10.
2: Unload at address 1, 2, 3.
3: Load at address 11.

7. The Buffer Memory Load Unload Logic

7.1 Function

The Telemeter Magnetics Buffer Memory (See Fig. 3), as explained in section 6, has its own internal logic which takes care of the necessary timing and addressing once it has received a load or unload command from the H.P.D. Whether it is wanted to load or to unload is entirely up to the external device, provided that it makes up its mind and does not try to do both at once.

A load demand ("READY-LOAD") will occur every time a word has been strobed into the XY-register. (See Fig. 6 and "Logic Master Diagram", H.P.D. - E - 001). This might be a Y, X or W-coordinate, and we do not know beforehand when it will happen.

An unload demand ("READY-UNLOAD") will be caused by the rising edge of the "READY-READ"-signal. (See Fig. 3 and 4).
Evidently, a load or unload-demand can arrive at any instant during the scan; it can happen that they come at the same time, or that a load is demanded at a time when the Buffer is unloading or vice-versa.

The Buffer Memory has a certain capacity; 128 words (16 bits each). If we try to store more than that the memory will "overwrite" coordinates which are waiting to be transferred to the computer, and they get lost. A book-keeping system which keeps track of the number of occupied addresses in the memory at any instant is therefore essential. The same system will also be able to tell us when the memory is empty; we do not want to waste computer time by transmitting words consisting of nothing but zeros.

The logic circuitry which deals with these problems has been named the "Memory Load-Unload Logic" (Schematic H.P.D. - E - 005) and the "book-keeping" logic the "Memory Control Counter" (H.P.D. - E - 003).

Before we start the explanation of the circuitry, let us summarize the different functions we want these two sections of the H.P.D. to execute:

1. Remember a load demand and execute as soon as the Buffer Memory is free.

2. Remember an unload demand and execute as soon as the Buffer is free.

3. If both load and unload are waiting, the load shall be given the priority.

4. The load demand is executed by giving a LOAD-PULSE (L) on the appropriate Buffer input line. The unload demand is executed by an UNLOAD-PULSE (U). Between two LOAD-PULSES or a LOAD and an UNLOAD-Pulse there must always be at least 5 microseconds.
5. A DDD-strobe must be transmitted to the DDC each time a word has been established on the Data Bus, that is a predetermined time after an UNLOAD-PULSE.

6. UNLOAD-PULSES must be inhibited when the Buffer Memory is empty.

7. If the Buffer Memory runs full all further commands must be inhibited and a warning light turned on**.

* The time between two unload demands is always much longer than 5 microseconds due to the computer.

** The flow of information to the computer can only be reestablished by human intervention. It is, however, very likely that overflow is caused by technical or human error, and not by a too dense picture.

Most of these conditions are solved by trivial digital circuitry, but point 5 has to be given special attention, especially for the case where the load and the unload-demand arrive at the same or slightly different instants. The Logic must then take a decision to execute one or the other, but not both at the same time.

7.2 The different Elements of the Logic

The L-U logic consists of the following main elements (See Logic Master Diagram H.P.D. - E - 001):

The two "Memories" for the load and unload demands, namely FF-XY and FF-R. An electronic switch consisting of the Flip-Flop FF-LU and the "AND" gates D12W and T, which will route a SYNC.-PULSE to the LOAD or UNLOAD output channel. A SYNC.-PULSE-generator triggered by a "Clamped Clock"; the output of which is connected to one of the output lines through the electronic switch described above. The INHIBIT-single shot which blocks the SYNC.-PULSE-generator for 5 microseconds after it has been fired, and finally a DELAY LINE which has been chosen so that the output switch had had time to settle before the SYNC.-PULSE arrives.

.../...
If special precautions had not been taken, it would be possible for say a load demand to release a SYNC.-PULSE, and before the 5 ms INHIBIT has blocked the input, a second pulse could have been triggered by an unload demand arriving just after the load demand.

The generation of such a double pulse is prevented by means of the "Clamped Clock". This is a DEC free running multivibrator ("Clock") which has been modified in a way such that it can be started or stopped by means of a DC-input signal. When the input level is negative, the clock is "clamped" in one position, and no output pulses can be generated. If the control signal goes positive, it will start oscillating, generating its first pulse after a delay which is equal to one pulse repetition period. (See oscillograms D4T, D7K and D7E on drawing HPD-E-001 as well as Fig. 9)

The repetition frequency has been set to 2 Mc/s, which is so low that the INHIBIT-pulse arrives well before the next pulse is generated.

7.3 The LOAD-process

Let us consider the case where a track-center coordinate has been detected and its coordinate stored in the XY-register as described in section 5. We shall assume that the Buffer Memory is ready and not full.

A load demand, namely the READY-Y pulse will arrive at the input X of the "AND" gate D3Z (See H.P.D.-E-001). Provided that we are "activated", the READY-LOAD flip-flop will be set.

This will release the CLAMPED-CLOCK, and a DEC fast pulse is generated 0.5 microseconds later. The pulse will:

a) trigger the SYNC.-PULSE-GENERATOR,

b) generate a DEC slow GATE PULSE at D9M.

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The GATE PULSE will flip the FF-LU to the load position, which means that "AND" gate D12W is enabled. 0,8 microseconds later the delayed SYNC.-PULSE arrives, and passes through the gate, via the level amplifier D16Z on to the Memory load command line.

In the meantime the 5 μs inhibit pulse has been generated, thus preventing further SYNC.-PULSES from being generated before the Memory has loaded the track-coordinate which was established on the input buses.

Once the LOAD-PULSE is generated it merely remains to reset the FF-XY as well as the XY-REGISTER. For this purpose, a LOAD-END PULSE is triggered off the trailing edge of the LOAD-PULSE, and passed through the "AND"-gate C5T * to the FF-XY and XY-REGISTER "clear" inputs.

Provided the Memory is waiting, it takes approximately 3 microseconds to execute a load demand, from the instant when READY-XY arrived until the FF-XY is reset (See Fig. 8).

If now a new load demand is given immediately, the CLOCK will not be released until 1,5 microseconds later when the 5 microseconds INHIBIT has timed out.

Each time we load the Memory we have to inform the "book-keeping" logic, which mainly consists of an up-down counter, named "Memory Control Counter" (H.P.D. - E - 001 and 003).

When loading we must count up. The M-counter UP-DOWN LOGIC is therefore set to "UP" at the leading edge of the LOAD-PULSE, 0,8 microseconds before the LOAD-END-PULSE triggers the counter input at pin C13R.

7.4 The UNLOAD-process

As described in section 3, the Computer gives a READY-READ each time a new word is wanted from the H.P.D. The rising edge of this signal will set the READY-UNLOAD flip-flop provided the Memory is not full**. From this point on, the process will proceed in the

---

* The function of C5T is described in the detailed description of the X-strobe Logic. During the LIGHT-period, this gate is always enabled.

** It might seem strange that it has been chosen to inhibit the UNLOAD as well as the LOAD process when the memory runs full. The reason is that we want to freeze the memory content to be able to find out exactly where on the picture the overflow happened.
same way as described for the LOAD-case, which means that after a minimum of 3 microseconds the Memory will receive an unload command.

As already explained in section 6, the demanded coordinate will be established on the Buffer Memory output buses 5 ms later. We want to free the Memory as quickly as possible. An external Buffer register (B) has therefore been placed between the T.M. Memory and the DDC (the level Amplifiers L.A. have no logic function). 5 microseconds after the UNLOAD-PULSE a sampling pulse strobes the word into the Buffer Register, and the T.M. Memory is ready for a new command. The 2 microsecond delay between the AB-STROBE and the leading edge of the DDD is necessary to allow the Buffer Register and Level Amplifiers to establish their correct potentials before the information is strobed into the DDC Data Register.

Note that the Buffer Register B is cleared before the AB-STROBE arrives. This means that the last word transmitted will always remain in the Buffer Register B, and can be checked on the visual display.

7.5 Explanation of the complete MEMORY LOAD UNLOAD LOGIC diagram

(H.P.D. - E - 005).

The previous explanations given above, with reference to the LOGIC MASTER DIAGRAM will enable the reader to recognize most of the elements on schematic H.P.D. - E - 005. The entire circuitry is built up from DEC modules, and a certain knowledge of the DEC logic system and the different building blocks is essential for the understanding of this schematic (See Ref. 6).

* All important signals and the contents of all the registers are visually displayed by means of fluorescent triodes DM 160.
To enable the reader to follow the operation from input to output, a series of oscillograms are presented on Fig. 8, which represent the UNLOAD process. The LOAD is practically identical.

As far as the logic operations are concerned, point 3 and 4 listed in section 7.1 above, need no further comment.

A few details will be clarified:

The READY-READ signal which is -28V DC when off, and +8V DC when on is shaped and changed to H.P.D. levels by Philips Digital Blocks before it enters the L-U-LOGIC unit.

For test purposes, a manual load or unload command can be given (points D4Y and D4Y) from Philips Schmitts triggered by push buttons located on the "Memory Control Panel".

The FULL and EMPTY inputs pass through toggle switches located behind the front panel, which are used for certain tests.

The 5 µs blocking pulse is produced by mixing the 0,8 µs SYNC.-PULSE and 4,2 µs INHIBIT in an "OR"-gate (D6L), merely to allow the single shot D1L to recover between succeeding SYNC.-PULSES*.

At the output of the DELAY LINE emitter follower (D1F) the SYNC.-PULSE is down in amplitude and needs to be reshaped. Therefore two fast inverters (D6W and Z) have been inserted in front of the OUTPUT GATE.*

The inverters D20H and L as well as D20P and T serve the same purpose.

7.6 Test results

Thorough tests have been made by means of specially constructed test-generators which simulate the on-line computer.

* see appendix 4.

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The most critical situation for the L-U logic operation is not the one occurring when a load and unload demand are given simultaneously. (This will give first a LOAD-PULSE and then 5 usec later an UNLOAD-PULSE).

The most critical case is when an unload demand arrives first, and then about 0.5 usec later, after the GATING PULSE (D6M) has been generated, a load demand switches the FF-XY to the load position. The LOAD-UNLOAD flip-flop will now be triggered by two split pulses, one on D4L and one on D4H. Being a regenerative element it is bound to settle in one position or the other, after a certain time, and we do not care which one it will be, as long as the OUTPUT GATE levels have been established before the SYNC.-PULSE arrives. This is the reason why it is necessary to delay the SYNC.-PULSE relative to the GATE PULSE.

To check that the DELAY LINE had been chosen correctly, a double pulse generator was used to produce the load and unload demands. The delay between the two was adjusted to simulate the worst condition and the oscillograms show that there is sufficient margin to insure correct operation for all possible cases (See Fig. 8).

8. The X- and W-Coordinate Digitizing Process

8.1 Problem

One will recall that the flying spot scanning cycle consists of a LIGHT-PERIOD of 6.5 usec and a "DARK-PERIOD" of 1 usec. During the LIGHT-PERIOD, the Y-coordinates of the tracks covered by one scan-line are detected and stored in the computer memory. The stage carrying the film moves with constant speed in the X-direction during the whole scan-period. This speed can have different but discrete values, up to 40 mm/sec. The X-coordinate is determined using the Ferranti MOIRE FRINGE System, the output of which gives a pulse every 2.54 microns (or with a finer grating system 1 micron) of travel. Assuming a 1 micron system we get 25 usec between pulses when travelling at 40 mm/sec which is the greatest speed envisaged*. These pulses are counted by a 17 bit binary

* The speed is limited by the driving mechanism of the table (in our case a lead screw with a servo-motor drive). A hydraulic system would possibly provide a greater speed range but would be more expensive.
forward-backward counter, the so-called X-(or for the 90° shifted scan W-) counter, which is built up from Philips digital building blocks, using well-known methods.

The content of the X-counter must be transmitted to the 709-computer at certain intervals, to keep track of the film-stage position. It was decided that this transmission should take place once each DARK PERIOD.

A certain feature of the computer program demands that 8 identical X-coordinates be transmitted to the 709 memory in succession and that each of them should be fitted with an 18th dummy-bit "1" (See appendix 1).

The problem is consequently to transmit, at a given moment during the DARK-period, the contents of the X-counter into the XY-register and load the Buffer-Memory (T.M.) 8 times in succession with this word. The DDC will at a later stage transfer this group of 8 identical words into the computer core-store.

8.2 The X-strobe Time Diagram

We define as "X-strobe" the pulse that enables the X:"AND" gates, transmitting the X-coordinate into the XY register. The X-strobe occurs only once each DARK PERIOD.

The X-strobe must arrive:

a) after the full grating count* has been cleared out of the XY-register,

b) never when the X-counter is counting.

The first condition is easily fulfilled, simply by waiting long enough after the DARK-PULSE. However, the second condition gives rise to a complication, because the X-counts and the DARK-PULSES are not synchronized in any way.

* See section 5.4
The time-diagram shown on Fig. X1 contains all the Buffer Memory (T.M.) LOAD-PULSES which take place during the DARK-PERIOD, as well as the logic information necessary to generate them. The right hand column will enable the reader to find the location of the signals on the schematic diagrams H.P.D. - E - 002/004 and on fig. X2.

The X-strobe process is started at the end of the CLEAR-Y-COUNTER pulse. As far as the Y-counter is concerned, this pulse can have any duration between approximately 5 μs and 0,99 ms. The DEC delay unit (Position A21) gives a standard pulse at the end of this time, and in our case it is set to give the end-pulse a few microseconds after the full grating count has been cleared from the XY-register.

The X-count (which is the trailing edge of a Philips Single Shot Pulse) is delayed by a time T1 relative to the real Ferranti pulse, mainly to allow 5 μsec for the forward backward line of the X-counter to settle if the direction has changed (See schematic H.P.D. - E - 038). This real Ferranti-pulse is also used to trigger an inhibit-pulse (FI) the purpose of which is to inhibit the X-strobe when the X-counter is counting. The X-count and inhibit pulses are shown in more detail on time diagram X2. The X-count and FI pulses are drawn in an arbitrary position on diagram X1. A detailed investigation of the different possible time-relations between FI and Y-CLEAR-END will be carried out below. We now proceed to the design of a logic system that fulfills the points a) and b).

8.3 Basic Logic Diagram of the X-strobe System.

Point a), namely generating a pulse which tells that the XY-register is ready to accept the X-coordinate, is settled above. We can use the Y-CLEAR-END pulse without further gating.

Point b) demands a system which upon request first checks whether the inhibit-pulse FI is present or not at that instant. If FI is not present, the X-STROBE should be generated at once, that is within a delay which is shorter than the so-called Prewarning Time T1. If FI is present, an "auxiliary" X-STROBE must be generated after the inhibit is over, but before the next one arrives.
The principle of the X-strobe logic is shown on the schematic diagram H.P.D. - E - 011. SW is a switch commanded by the relay-coils S (Set) and R (Reset). The first pulse arriving is the RESET one which pulls the switch into the lower position, connecting the output to the delay DA. When the input pulse arrives it will throw the switch to the upper position, provided the AND-gate A is not inhibited by an FI pulse. Let us first assume that A was enabled when the input pulse arrived. An X-strobe will be transmitted at a time given by the delay DN. This delay ensures that enough time has elapsed to allow the switch to pass from DA' (See footnote) to DN and settle in the new position, and is of course necessary whether SW is a mechanical or an electronic switch.

If the gate A was inhibited when the input pulse arrived the switch will remain in the RESET position, and the X-strobe will be transmitted at a time given by the delay DA'. Note that in either case we know approximately where the next X-count will be placed; in the first case (FI) not before 7 μs have elapsed, and in the second case (not FI) maximum 7μs later. The critical situations are sketched on the time diagram Fig. X2 and will be treated in detail.

**Case 1**  
The input pulse (which is identical to Y-CLEAR-END) arrives just before the gate A is inhibited by FI. The switch is thrown to the DN position and we get a "normal" X-strobe out DN μs later. Evidently, DN must be long enough to allow the switch to settle, but not so long that the X-strobe will arrive at or after the X-count. That is: a) DN longer than the settling time which is approximately 0.2 μs. b) DN shorter than T1 = 7μs.

**Case 2**  
The input pulse arrives just after the gate A was inhibited (FI). The switch remains in the RESET position and the "auxiliary" X-strobe is transmitted DA'μs later. DA' must then be long enough to allow the X-counter to settle, that is DA' longer than (T1 + T2) = 14μs*.

* In the actual circuit the delay DA is triggered off the trailing edge of DN, thus DA' = DA + DN. The time diagram on fig X2 refers to the schematic H.P.D. - E - 016.
Case 3 The input pulse arrives when the gate A is inhibited, but close to the trailing edge of the inhibit (FI) pulse. DA must then be short enough to transmit the "auxiliary" X-strobe before the next X-count, that is DA' shorter than \((25 \mu s - T2) + 18 \mu s\).

The borderline-case between 1 and 2, where the input pulse arrives at the same instant as the FI leading edge does not produce a split X-strobe due to the delay DN which is long enough to allow the switch to settle in one position or the other, before the output pulse is generated. The principle described above is easily transferred to a fully electronic circuit, and in our case the delays were set to be:

\[
DN = 2.5 \mu s  \\
DA' = 16.5 \mu s (\text{Yielding } DA = 14 \mu s)
\]

These will be seen to satisfy the above conditions.

8.4 Description of the complete 8X-strobe Circuit

The circuit is drawn on H.P.D. - E - 016. Some of the units have been designated, such as FF-SW, DN etc. The ones which have not been fitted with a "name" are referred to by means of the block number and the output pins, thus the AND gate on schematic H.P.D.-E-016 with the inputs Y-CLEAR END and FERR. INHIBIT is referred to as C 5 H.

The X-strobe logic has two separate functions:

1. To strobe the coordinate contained in the X-(W) counter into the XY-register, by pulsing the AX AND-gates at a given moment.

2. To control the LOAD-UNLOAD logic in such a way that the X-coordinate temporarily stored in the XY-register is loaded into the buffer memory (TM) 8 times in sequence.

Part 1 is the electronic equivalent to H.P.D. - E -011. The switch SW is composed of the flip-flop FF-SW plus the AND-OR gate C5L (P). The delays DN and DA, are DEC delays, 4301 which give standard DEC-pulses at the end of the preset times. C3P and C3Z are AND-gates which route the strobe-pulse to the AX or AW gates according to the polarity of the N-S signal (normal or 90 degrees shifted scan; (See Ref. 4).
As one single Pulse Amplifier is able to drive only 16 AND-gates 4113, the load of the 16 AX-AND gates is shared between two such amplifiers, namely C7J and C7E. The latter is also connected to the XW-input of the READY-LOAD Flip-Flop of the LOAD-UNLOAD Logic.

As one will recall from the description of the Buffer Memory L-U Logic, a LOAD-PULSE will be given 2.7 µs after the Ready-Load Flip-Flop was set (if the memory is not unloading at that instant). Due to the technique of using a "Clamped clock" this will be repeated every 5 µs if the Ready-Load Flip-Flop is not reset.

Part 2 of the X-strobe logic now contains the elements that control the L-U logic in such a way, that the XY-register is strobed 8 times, instead of once, once the X-strobe has occurred at the Pulse amplifier output C7E.

Normally the Ready-Load F.F. is reset by the LOAD-END pulse which occurs at the trailing edge of the 0.8 µs long LOAD-pulse (see Fig. 8, series 2). The same pulse is used to clear the XY-register. Simply by suppressing this clear-pulse, the Load-Pulses will be repeated every 5 µs, and the XY-register will not be cleared.

This suppression takes place in the AND-gate C5T which is controlled by the last stage of a 4 bit counter, named the CC-counter.

During the LIGHT-period CC-4 is in the "set" position, and the gate C5T is enabled (see also appendix 3). Reset of CC takes place at the beginning of the 8X-strobe process, when the Y-CLEAR END arrives. This means that the AND-gate C5 is inhibited well before the first X-load pulse arrives. After 8 Load pulses CC-4 is again in the "set" position, and the LOAD-END-pulse which follows 0.8 µs later (the transition of the C-counter is much less than 0.8 µs) will stop the Load process and clear the XY-register. At the same time CC-4 will inhibit the C-counter input gate (C5W) to prevent further Load-Pulses (during the following LIGHT-period) from triggering the counter input. The state of the counter is now (written in binary) 1-0-0-0 and it remains like that until the next CC-clear pulse arrives.

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8.5 Test-results of the 8X-strobe Logic

A double pulse generator was built to test the 8X-strobe logic. By synchronizing the X-count (Ferranti-count) with the Clear-Y pulses the critical situations shown on the time diagram X2 could be simulated.

As the delay DN (H.P.D.-E-016) had been set to 2.5 μs, which is around 10 times longer than the settling time of the PP-SW, no split pulse occurred and the logic worked as expected.

Fig. X4 shows some of the actual oscillograms photographed during the test.

9. Start-Stop Logic, Stage and Film-control

As described earlier, the DDC wants an "Interrupt" signal at the beginning of a scan and an "End of File" (E.O.F.) at the end.

The "Interrupt" must not be given until the mechanical stage has reached constant speed, and is timed by the Y-CLEAR-END pulse, which also starts the 8X-strobe process.

The Start Stop logic is part of the Stage and Film-control logic which is being constructed at present. This will be described in a later report. (See Ref. 2, 3 and 6)

10. Power Supply and Control

For the Prototype, electronically regulated transistorized power-supplies were used. For the final version it is intended to use simpler supplies with saturating transformers for the digital circuitry.

The Power Control Unit has a logical system which permanently checks the different voltages, and disconnects the H.P.D. if any of them fails or reaches a value which is set to be ± 10 % of the normal one.

11. Final Remarks

The digital circuitry described in this paper was specifically designed for a system where the density of measured data is so high, that it is necessary to compute while measuring. Where this is not necessary, as would probably be the case if an H.P.D. type machine were to be used to measure spark-chamber pictures, the possibility exists to transfer the data to magnetic tape using very much the same logic as for the present system.

* This circuitry was designed, built and tested by R. Zurbuchen.
ACKNOWLEDGEMENTS

I would like to thank Dr. L. Kowarski and Dr. Y. Goldschmidt-Clermont, for their support of the work of which this report describes a part.

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Finally, I am particularly indebted to R. Zurbuchen, and K. Zumbrock for their part in the construction and checking of the circuits, and to Paul Hough and Brian Powell for their help in preparing this report.
Appendix 1

The computer must be able to distinguish between an X (or W) and a Y-coordinate. The maximum number of bits of a Y-coordinate is 15. The corresponding figure for X(W) is 17. If one adds a dummy-bit in the 18th position to the X-coordinate, this bit always being a "1", the X-coordinate is "marked". By looking at the 18th bit of every coordinate stored in the 709-memory, the computer can now find an X-coordinate and sort it out from the Y's. This is rather time-consuming; one therefore transmits a group of 6 (equal) X-coordinates to the computer memory at a time. These coordinates will be stored in the addresses, say n to n + 7. Now the computer only has to look at every 8th coordinate to find one of the X's, since it is bound to hit one of the 8 X's in the group. The conclusion is therefore that we want to transmit a group of 8 equal X's each DARK-period instead of a single one.

Appendix 2

From the 8X-strobe-logic point of view the prewarning time T1 must only be longer than DN, which is determined by the transient response of FF-SW and the AND-OR gate C3P. DN is made 2,5 µs, which is the shortest time one can get from a DEC 4301. Actually, 0,5 µs would be ample, and this could for instance be obtained by means of a delay line. In this way the time between the Ferranti pulses could be made even shorter than 25 µs, if wanted. One would, of course, have to generate the FI-pulse by means of a 3rd single-shot, to make the prewarning-time T1 approximately 1 µs instead of 7 µs.

Appendix 3

One might ask what happens at the beginning of a picture. Assume that we make no special provision for setting the C-counter in the 1-0-0-0-state when the apparatus is switched on. Due to the Start-Stop Logic, (see section 9), no LOAD-pulses will occur before the signal ACTIVATE is given. ACTIVATE is triggered by the Y-CLEAR-END pulse, the same signal as is used to clear the CC-counter. Thus we have the same situation as already described: the T.M.-memory will first be loaded 8 times with the X-coordinate contained in the X-counter, and the first words transferred to the 709 computer will be these 8 X-coordinates.
Appendix 4

Recently DEC has developed a few new modules which could simplify the logic in certain places. Merely for this reason it is proposed to make some minor modifications on subsequent HPD models.

These new DEC modules are:

1. "Integrating Single Shot" DEC 4303. This unit has among others the following features:
   a) It has no recovery time.
   b) It can be repeatedly triggered and the delay will continue for the specified duration after the final triggering.

2. "Pulse Amplifier" DEC 4604.
   This Pulse Amplifier has regenerative features which make it suitable for standardizing 0.4 μs pulses. It can in some cases, be used instead of a Schmitt or a Pulse Amplifier DEC 4603 with feedback.

The modifications proposed would be:

1. The Delay 4301 position Dll could be replaced by a 4303.
   The inhibit OR-gate D6 - H,L could then be left out thus saving two inverters.

2. The Pulse Amplifiers 4603 in position D9-J and D9-E could be replaced by 4604 and fed directly from D12-W and D12-T saving 4 inverters. Another solution would be to use the 4603, but include feedback for better pulse restoring. (The present scheme has so far given no trouble, but needs more components than the solutions proposed here.)

3. The Delay 1304-2 position A9 with its adjacent Delay Line and OR-gate could be replaced by a 4303 and driven from the Track Center Flip-Flop position All directly using negative going level change for triggering. This would save: 1 Pulse Amplifier, 1 Delay Line and 2 Inverters.

4. The modified Delay 1304 position A10 could be replaced by a 4303. The Pulse Amplifier A15-K would have to be replaced by a normal 4603 with feedback. (So far, the present scheme has given no trouble, and no components would be saved. However, one would not have to modify any DEC-modules for the new circuit.)
REFERENCES


5. IBM Special Features Bulletin. "Direct Data Connection for IBM 709 RPO 80979".


FIGURES

Fig. No.
1. Basic System Diagram
2. Scheme to derive Flying Spot
3. Basic System of Computer Connection
4. Time Diagram of Operation with Computer via D.D.C.
5. Oscillograms of Track and Grating Signal
6. Basic Principle of Y-Digitizing
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FIG. 2

scheme to derive flying spot
MAIN PROGRAM

INTERRUPT FROM HPD

RESET DATA-REGISTER

CHANNEL B READY READ TO HPD

D. D. DEMAND

DATA REGISTER

B-CYCLE

WORD COUNT

TRANSFER OF DATA TO COMPUTER CORE STORAGE

T1 : DEPENDING UPON PROGRAM
T2 : DEPENDING UPON THE PICTURE
T3 : LESS THAN ONE IBM CYCLE
     (ONE CYCLE = 12 MICROSECONDS)
T4 : DEPENDING UPON PROGRAM :
     MAX. 5 CYCLES

* ALL IN MICROSECONDS

NOTE : RISE-TIMES NOT INCLUDED ON DIAGRAM.
From top:

TRACK SIGNAL

1 ms/cm  5V/cm

TRACK SIGNAL expanded

20 µs/cm  5V/cm

SINGLE TRACK* and
its integral (top)

5 µs/cm  2V/cm

GRATING SIGNAL

5 µs/cm  5V/cm

GRATING SIGNAL

20 µs/cm  5V/cm

* Minimum ionizing track from BNL 20 inch Hydrogen Chamber. Note the good signal to noise ratio due to improved experimental optical system (R. Palmer).
A3J : TRACK CENTER PULSE
A11R : TRACK CENTER flip-flop
A3E : FIDUCIAL PULSES

A11R : TRACK CENTER flip-flop
A12E : CLOCK OUTPUT
A18E : READY-Y PULSE
1 \mu s/cm 5V/cm

A3E : FIDUCIAL PULSES
A10K : DARK SIGNAL
generator input

A10J : DARK LEVEL
A18M : Y-CLEAR-START
5 \mu s/cm 2V/cm

Y-Digitizing Process and DARK signal
generation (Schematic HPD-E-002).

Fig: 7
Series 1: From top:

D3R : Unload Demand

D4T : RDY-UNLOAD flip-flop

D7K : CLOCK input

D7E : CLOCK output

D7E : CLOCK output

D9M : GATING PULSE

D12S : OUTPUT GATE level

D12Y : DELAYED SYNC. PULSE

0.5 μs/cm  2 V/cm

Series 2: From top:

D12T : UNLOAD-PULSE

D9E : UNLOAD-END-PULSE

D15J : DDD-Strobe

D4T : RDY-UNLOAD flip-flop

2 μs/cm  5 V/cm

Buffer Memory LOAD-UNLOAD-LOGIC:
Time diagram of unload process.

Fig: 8
Fig. 9. Two photographs from the CERN 30 cm. hydrogen bubble chamber showing events typical of what one wishes to measure with the B.P. D.
Fig. 10. The upper photograph shows the two racks of electronics described in this report. The right-hand one contains the power supplies and test circuitry. The other contains the buffer memory, the analogue and logical circuits. The lower photograph is a general view of the mechanical and optical system used for the preliminary tests.
Fig. 11. The upper photograph shows the sub-chassis which contains the X counter. The lower one shows on the right the level amplifiers which drive the DDC cable and on the left a DDC building block.
NOTE: The diagram is unchanged when W-coordinates in stead of X.
X-COUNTER : FORW. BACKW. LINE

FI = INHIBIT PULSE TO X-STROBE INPUT "AND" GATE

X-COUNTER INPUT. COUNT AT POS. GOING EDGE.

Y-CLEAR-END PULSE = START OF X-STROBE LOGIC**

X-STROBE FOR CASE 1

X-STROBE FOR CASE 2

X-STROBE FOR CASE 3

* ALL IN MICROSECONDS

** TO SIMPLIFY DIAGRAM, X-COUNT IS USED AS REFERENCE AND Y-CLEAR END DRAWN IN THE 3 CRITICAL POSITIONS. DA IS TRIGGERED OFF DN FOR CONVENIENCE.
Objet: H.P.D. X (W) COUNTER LOGIC
Subject: BLOCK-DIAGRAM

NOTE: CIRCUITRY FOR SHIFTED SCAN (W) IDENTICAL

FIG. X3
Picture X-01: From top:
C3F: Y-CLEAR-START
C5F: FI inhibit pulse
C5E: Y-CLEAR-END
C4J: FF-SW
C5K: Output Delay DN
C7E: X-Strobe pulse
10 microseconds/cm
Normal X-Strobe

Picture X-02: From top:
C2J: Clear CC-counter
C5U: Memory LOAD pulses
C8Z: First bit CC-counter
C8J: Last bit CC-counter
C5S: LOAD-END pulses
C7M: Clear XY-register
10 microseconds/cm
and same trigger as above

Picture X-03: From top:
C3F: Y-CLEAR-START
C5F: FI inhibit pulse
O3S: X-count
C5E: Y-CLEAR-END
C4J: FF-SW
C7E: X-Strobe pulse
5 microseconds/cm
Note: the normal strobe is inhibited and the auxiliary one gets through.

HPD: 8X-Strobe Logic: oscillograms from final circuit XS-3a.

Fig. X4
NOTE: Delay A10 triggered (pas fast dec.) during light period. Time set to >2X5.4μd
J. output remains neg. until 10μd after last fid. pulse.
DELAY DN SHORTER THAN DA

THROW SWITCH IF A NOT INHIBITED

INHIBIT PULSE FROM X-COUNTER LOGIC

F1

DELAY DN

A

AND

INPUT PULSE

(AT A GIVEN TIME AFTER DARK-PULSE)

RESET

(RESET BEFORE INPUT PULSE)

X-STROBE

OUT

SW

SWITCH DRAWN IN RESET POSITION

R

S

PRINCIPLE OF 8X-STROBE

LOGIC
INHIBIT AND COUNTER
INPUT DELAY

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