FTK: A HARDWARE REAL-TIME TRACK FINDER FOR THE ATLAS TRIGGER SYSTEM

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FAST TRACKER (FTK) IN THE ATLAS EXPERIMENT

Example:
R-phi view of Barrel region:

3 PIXEL layers

Track crosses 11 detector layers

4*2 SCT layers

Total # of readout channels:
PICTELS: 80 millions
SCT: 6 millions
+ IBL: 6 millions @ 3cm
At hadron colliders:
- **Common problem:** identification of particle tracks in vertex detector

Huge amount of produced data
- **Limited amount of events can be transferred**

Data reduction must be performed

Trigger system
- Particle track recognition in real time
- CPUs of HLT not suitable for this task
Pattern recognition problem can be solved by an Associative Memory (AM) chip.

- Integrated circuit
- Content Addressable memory
- Maximum level of parallelism
- Comparison of input data with a set of precomputed patterns stored in a memory
- Select few tracks among several tracks

1990: AM chip v.1 – ASIC CMOS 700 nm with 128 patterns
1998: AM chip v.2 – FPGA same of AM chip v.1
2004: AM chip v.3 – ASIC CMOS 180 nm with 5000 patterns
THE AM CHIP ARCHITECTURE

For each bus and for each pattern there is a small CAM cell array (layer x)

- It compares its own content with all data received. If it matches a memory is set (FF)
- The partial matches are analyzed by the majority logic and compared to the desired threshold
- A priority encoder (Fischer Tree) reads the matched patterns in order

The AM and commercially available CAMs differs substantially

- store partial matches
- find correlations at different times
FAST TRACKER (FTK) INSIDE ATLAS

FTK is an electronic system able to find and reconstruct particle trajectories in ATLAS.

FTK looks at 12 logical layers:
- 4 pixel layers including the new Insertable B-layer (IBL)
- 8 Silicon Microstrip Trackers (SCT) layers corresponding to 4 axial and 4 stereo sides

FTK targets to reconstruct all tracks with $p_T > 1$ GeV, given a positive L1 decision.

Its handling of a 1 billion of patterns of data with a large number of ASICs and boards.

FTK is a **massively parallel system** that could manage input data from 64 $\eta - \phi$ towers.
FTK ARCHITECTURE

**Hits:** positions of pixels are given to the DF boards
The Data Formatter (designed in Fermilab) reorganizes the incoming data from the pixel and strips RODs.

The IM is installed on the DF and it finds clusters.

Two different board designs:

- a first board designed in Waseda (Japan) with a Xilinx Spartan-6 FPGA
- a second board designed in Frascati (Italy) with a Xilinx Artix-7 FPGA
DATA FORMATTER (DF) AND INPUT MEZZANINE (IM)

The Data Formatter (designed in Fermilab) reorganizes the incoming data from the pixel and strips RODs.

The IM is installed on top of the DF and it finds clusters.

Two different board designs:

- a first board designed in Waseda (Japan) with a Xilinx Spartan-6 FPGA
- a second board designed in Frascati (Italy) with a Xilinx Artix-7 FPGA

All the 36 boards have been integrated in Advanced Telecommunications Computing Architecture (ATCA) crates within the ATLAS experiments and are fully functional.
FTK ARCHITECTURE

Cluster positions are given to AUX boards
AUXILIARY CARD

The AUX card is installed in the rear of the VME crate.

It receives and organizes the hits from DF for pattern matching.

It receives track roads and performs the first stage of track fitting.
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It receives and organizes the hits from DF for pattern matching.

It receives track roads and performs the first stage of track fitting.

Starting from February 2016, all the 16 AUX cards will be mounted.
Super strips are cluster positions at coarse granularity and are given to AM boards/chips for the pattern recognition.
AM BOARD (AMB)

The AMB performs pattern recognition

It spreads input to the AM chips in parallel

It collects roads

Bandwidth to chips: 100 GB/s

Power consumption: 250 W
The AMB performs pattern recognition. It spreads input to the AM chips in parallel. It collects roads bandwidth to chips: 100 GB/s. Power consumption: 250 W.

- **early 2016**: testing of the latest prototypes
- **end of 2016**: installation of 16 AMBs
- **early 2017**: installation of 32 AMBs
- **2018**: complete with all the 128 AUXs and AMBs
### ASSOCIATIVE MEMORY (AM) CHIP

- **The AM is the core device of FTK**
- **Used for the pattern recognition task**
- **Based on XORAM cells**
- **Memory depth: 128 kpatterns**
- **It compare 1.6 Pbit/s**
- **Serializer and Deserializer up to 2.4 GHz**
- **About 421 million of transistors designed in 65 nm**
- **7 power domains**
- **14 different CLKS**
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early of 2016: the AM06 chip has been extensively characterized

end of 2016: complete the industrial tests
**FTK ARCHITECTURE**

**Roads:** valid super strip combination found

**1st stage tracks:** fits using 8 layers are given to SSB
SECOND STAGE BOARD (SSB)

The SSB takes the roads from the AUXs and integrates these results with the 4 missing data layers.

Two different types of SSBs have been designed.

Both have identical Extrapolator (EXP) and Track Fitter (TF) functions, and different HW functions to perform duplicate 12-layer track removal that takes into account the $\eta - \phi$ overlap regions.
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The SSB has been tested in 2015.

Mechanical and electrical tests are ongoing.
2\textsuperscript{nd} stage tracks: fits using 12 layers are given to FLIC

FTK ARCHITECTURE

ROD \rightarrow DF board \rightarrow AUX board \rightarrow SSB board \rightarrow FLIC board \rightarrow ROS

- ROD: hits
- DF board: clusters
- AUX board: superstrips
- SSB board: roads
- FLIC board: 2nd stage tracks
- ROS: FTK tracks
The FLIC collects final track segments from SSBs.
FTK TO LEVEL-2 INTERFACE CARD (FLIC)

The FLIC collects final track segments from SSBs.

A first FLIC board has been installed at CERN.

In March 2016, the two FLIC boards will be integrated at CERN.
EXPECTED PERFORMANCE

Simulations have been performed at 46 and 69 average number of interactions per crossing.

The efficiency is 83% for tracks with $p_T > 1$ GeV and rises to above 90% for $p_T > 10$ GeV. Slight loss in efficiency for tracks with $p_T > 40$ GeV.
CONCLUSIONS

Presentation of FTK architecture and its expected performance

The current status of each subsystem has been provided

The FTK prototypes have been characterized

FTK system should be online from the fall 2016