The LHC high-luminosity upgrade will start after 2022 and will provide an instantaneous luminosity of approximately $7\times 10^{34}$ cm$^{-2}$ s$^{-1}$ to the ATLAS experiment. In order to handle this increased luminosity, ATLAS aims at integrating 3 ab$^{-1}$ in this phase. As of today, a full picture of the achievable analyses in this regime cannot be drawn. However, this upgrade will definitely give ATLAS access to large fractions of the SUSY phase space and will expand its Higgs physics reach.

The figure on the right shows a simulation of the expected observable signal in the ATLAS detector for the Higgs decay $H \rightarrow \mu\mu$ with a 7% or 3% S/B ratio or expected with 3 ab$^{-1}$ of integrated luminosity. In order to reach the required instantaneous luminosities, ATLAS will need to face challenging conditions: event pile-up, track matching. With a target of $0.3 \text{ ab}^{-1}$ for Run I and $10 \text{ ab}^{-1}$ for Run II, ATLAS access to large fractions of the SUSY phase space and will expand its Higgs physics reach.

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The ATLAS Trigger System

The ATLAS trigger and data acquisition system feeds off the detector’s front-end electronics and proceeds in two major stages. These correspond to the hardware (Level 1) and software (HLT: High-Level Trigger) steps of its trigger path. In Run I the High Level Trigger was organized in a two-level (Level 2 and Event Filter) pipeline. Upon event acceptance, the Level 1 primitives are communicated to the HLT as “Regions of Interest” (RoI). These identify geometrical sub-regions of the ATLAS detector that can be identified and read-out by the early 150 MHz stage without having to process the full detector information. In parallel to the trigger decision stages, data is read-out, merged and built into a single "event" entity and output to permanent storage. The ATLAS trigger will evolve into a much higher performance system by the end of Phase 2 upgrades.

ATLAS Detector Upgrades: Phases 0 and 1

The upgrade of the ATLAS TDAQ system will happen incrementally through the LHC upgrade phases. The just concluded Phase 0 has been characterized by the merging of the two HLT stages into one single entity, the inclusion of topological capabilities in the Level 1 trigger hardware and the improved pile-up suppression of the Level 1 calorimetric trigger hardware. In Phase 1 (2010), this suppression will be further enhanced by refining the granularity of the clustering algorithm (see figure to the right).

The ATLAS physics reach is being progressively enhanced through the LHC upgrade phases. Phase 0 the "extended Barrel" muon (1 SD$_{\text{global}}$-1 $\text{SD}_\text{track}$) trigger fake rejection will be improved thanks to the coincidence with muon identification in the hadronic calorimeter ("the Extended-Barrel" inset in the picture). A new Small Wheel muon detector will then be introduced in Phase 1, strengthening the fake rejection of the ATLAS forward muon calorimeters (TGC).

Phase II upgrades will face an average event pile-up of 200, and will provide a space and an equivalent time of space at the most of the layer of the detector equivalent to $2 \times 10^{10}$ neutrons/cm$^2$. Emphasis will therefore be on further reducing fake rates and improving detector resolution to maintain physics efficiency and maximize the hadronic energy resolution. The ATLAS software and computing infrastructure will have to be re-designed to cope with this regime, accompanied by the renovation of the L1 calorimeter, the muon drift chamber and the installation of additional shielding.

ITk: The ATLAS Inner Tracker for High Luminosity

The ATLAS inner tracker (ITk) will be completely replaced with a higher trigger extending to higher luminosities. It will be a full silicon-based device to allow the interception of charged tracks at most 14 points (Figure 6). The innermost layers will be based on $29 \times 29$ pixel elements (compared to the current $80 \times 80$ pixel elements of $50 \times 400$ $\mu$m). The outer ITk layers will be made of double-sided silicon strip detectors with $7.45 \mu$m spaced strips (at 40 mrad stereo angle) ranging in length from 2.45 cm to 4.9 cm, for a total of $\sim 74$ hits per track. ITk will be read-out at $150 \text{ kHz}$ rate.

ITk Readout Latencies

The strip tracker readout is based on the "ABC/103" ASIC, where a double-buffer architecture has been implemented to reflect the two hardware trigger levels. Upon L0 acceptance a RoI map identifies subsets of data from the Level 1 buffer which are read-out prior to Level 1 accept delay. Depending on the detector stage size and geometry, multiple ABC103 are linked to an Hybrid Chip Controller (HCC) in a star topology. Detailed simulations have shown that an approach with Regional strip identifier space per Level 1 accept delay, the use of a star topology (rather than daisy-chain), even the most occupied strip regions can provide R3 data for 10% of L0 accept delays within 6 $\mu$s.

ATLAS-TDR-02: pattern recognition is based on "associative memories", with each location corresponding to a coarse resolution pattern of "super-pixels" (the plots of hits of strips) on the ITk layers. Tracks are then filtered with a linear FPGA-based algorithm.

The number of associative memory locations needed has been studied by simulating Q1(100) single muons in a volume corresponding to about 1800 of ITk coverage. Studies based on the use of the strip detector information alone show that O(100) patterns is needed for full ITk coverage (adding up to 10 ATCA shelves based on ITk hardware performances). Many more details (use of pixel layers, detailed hardware design) are under study and will be defined in the coming months.

Off-Detector Processing

Studies have been performed so far mainly on the implementation of track finding and fitting based on the architecture and ASIC technology of the fast track trigger project [ATLAS-TDR-02]. pattern recognition is based on "associative memories", with each location corresponding to a coarse resolution pattern of "super-pixels" (the plots of hits of strips) on the ITk layers. Tracks are then filtered with a linear FPGA-based algorithm.

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ITk Readout Latencies

The ATLAS inner trigger (ITk) is capable of reducing the time for Level 1 decision. The resulting constraints for L1Track will therefore be:

- 24 $\mu$s total decision latency (L0A + L1A) subdivided in:
  - 6 $\mu$s for regional ITk readout requests (R3 or R3)
  - 12 $\mu$s for track identification/reconstruction
  - 6 $\mu$s for data propagation and global Level 1 decision

Can L1Track fit in this timing budget at HL-LHC occupancies?

Physics Performance

- ATLAS HLT will require a significant redesign of the ATLAS detector and TDAQ system.
- Better rejection at early trigger stages will be essential to cope with the harsh pile-up conditions.
- L1Track will provide essential rejection through hierarchical track reconstruction.
- ATLAS constraints of L1A = 400kHz and L1 latency > 30$\mu$s make the L1L1 approach unfeasible and the use of RoI-based L1Track possible.

Roll-less Approach

Instead of reducing data flow, an alternative approach is to introduce Double slice layers to identify track "strips" to be combined. This would reduce the scale of the single-layer hit combinations early in the track-finding stage, hereby spreading the data and moving the pattern recognition moves from single-layer hits to track stubs to full tracks. Effectively, the stub indication relative to the double-stripe system acts as an approximate measurement of momentum (“p-filtering”). Combining 2-3 strips introduces further p$\perp$ discrimination. To the non-negligible impact in the ITk design, a decision on this approach will have to be taken by Q1 2016.

Conclusions

- HL-HLC will require a significant redesign of the ATLAS detector and TDAQ system.
- Better rejection at early trigger stages will be essential to cope with the harsh pile-up conditions.
- L1Track will provide essential rejection through hierarchical track reconstruction.
- ATLAS constraints of L1A = 400kHz and L1 latency > 30$\mu$s make the L1L1 approach unfeasible and the use of RoI-based L1Track possible.
- ATLAS will use Regional strip identifier space per Level 1 accept delay.
- Full Pixel readout at 1MHz may add flexibility, but not studied yet.
- An ITk readout latency of 6$\mu$s seems achievable.
- First pattern recognition results, using Strips only, indicate that the FTK concept would work well also for L1Track at ATLAS