Pixel 2010: A rsum

Wermes, Norbert (University of Bonn)

11 September 2011

The research leading to these results has received funding from the European Commission under the FP7 Research Infrastructures project AIDA, grant agreement no. 262025.

This work is part of the following AIDA Work Packages:

9: Advanced infrastructures for detector R&D
3: Microelectronics and interconnection technology

The electronic version of this AIDA Publication is available via the AIDA web site [http://cern.ch/aida](http://cern.ch/aida) or on the CERN Document Server at the following URL: [http://cdsweb.cern.ch/search?p=AIDA-PUB-2011-005](http://cdsweb.cern.ch/search?p=AIDA-PUB-2011-005)
PIXEL 2010 – A Résumé

N. Wermes

Physikalisches Institut, Bonn University, D 53115 Bonn, Germany

A R T I C L E  I N F O

Available online 7 January 2011

Keywords:
Pixel detectors
Semiconductor detectors
Hybrid pixels
Monolithic pixels

A B S T R A C T

The Pixel 2010 conference focused on semiconductor pixel detectors for particle tracking/vertexing as well as for imaging, in particular for synchrotron light sources and XFELs. The big LHC hybrid pixel detectors have impressively started showing their capabilities. X-ray imaging detectors, also using the hybrid pixel technology, have greatly advanced the experimental possibilities for diffraction experiments. Monolithic or semi-monolithic devices like CMOS active pixels and DEPFET pixels have now reached a state such that complete vertex detectors for RHIC and superKEKB are being built with these technologies. Finally, new advances towards fully monolithic active pixel detectors, featuring full CMOS electronics merged with efficient signal charge collection, exploiting standard CMOS technologies, SOI and/or 3D integration, show the path for the future. This résumé attempts to extract the main statements of the results and developments presented at this conference.

© 2010 Elsevier B.V. All rights reserved.

1. Introduction

The first conference on pixel detectors in particle physics was held in 1988 in Leuven. During the past 20 years pixel devices have been developed to precise tracking and imaging detection devices, first as hybrid pixel devices, the technology of choice for the LHC and for new detectors for X-ray imaging at synchrotron light sources. The advances in CMOS technology have opened possibilities towards more monolithic or semi-monolithic devices, with trade-offs to be made between charge collection (full or uncomplete), the level of circuit integration (partial or full CMOS), and the level of 3D integration. As of today compromises must be made. That these approaches have matured is evidenced by the fact that non-hybrid technologies are chosen for the pixel vertex detectors of the STAR experiment at RHIC (CMOS active pixels) and of the Belle II experiment at superKEKB (DEPFET pixels). This demonstrates the current direction of the pixel development shown in Table 1 which compares particle rates and radiation levels are lower, non-hybrid pixel technologies are chosen, promising material budgets almost an order of magnitude lower than for the LHC.

For imaging applications, hybrid pixels have also been the prime choice so far, in particular since material considerations do not play a large role. Going from X-ray imaging and imaging at synchrotron light sources to the new demands at the X-ray laser sources (XFEL) in Stanford and Hamburg, the challenges are identified by (a) a huge dynamic range of photon flux (up to \(10^6\)), (b) high count rates per pixels (\(>\text{MHz}\)), (c) very large frame rates (\(\sim 5\text{ MHz}\)), and (d) little dead time and a ‘seamless’ architecture.

2. The LHC pixel detectors

To underline it: these are big pixel detectors: 2–3 layers/disk, roughly 1 m long (\(\sim 7\text{ m with services}\)), of the order of 10\(^8\) individually amplified channels. In my view the main message presented at this conference on the operation experience in LHC collisions with these big pixel detectors is [1–7]. They are essentially noiseless devices. With a noise hit level per pixel and bunch crossing below 10\(^{-9}\) after masking pathological channels and after reconstruction, less than 0.2 noise hits per event are observed [7]. Operated at modest threshold settings (\(\sim 3000\text{e}^–\sim 4000\text{e}^–\)), efficiencies above 99\% and trigger rate capabilities up to 80 kHz have been achieved. This must be considered a great achievement which resulted from many years of pixel R&D. The resolution of the charge measurement is excellent as is demonstrated for low momentum tracks (\(< 1 \text{ GeV}\) with large specific energy loss in Fig. 1(a). The only drawback that one can identify is the not so small amount of...
material that these trackers have, more than 3% of a radiation length per layer in the present trackers, still well above 1% for current sLHC designs. This is largely due to the fierce radiation environment at LHC requiring the hybrid pixel technology and the detectors to be operated at temperatures below 0°C, enhanced by the fact that they are a “first of their kind”. The ALICE pixel detector is an exception achieving a 1.1%/X0 per layer due to a dedicated effort in minimizing the material in all aspects. This is helped by the fact that for heavy ion collisions at LHC a homogeneous 4π coverage is not mandatory as it is for pp collisions. Therefore, the stiffness of the very thin support structure can be obtained by radial, chamber-type structure elements. Furthermore, the lower luminosity for heavy ion collisions results in less detector radiation damage which in turn allows to operate the pixel detector at room temperature saving cooling material.

An interesting aspect which is now seen with the first data is the effect of the different charge sharing tunings of ATLAS and CMS. ATLAS with 50 × 400 μm2 pixel cell dimensions has chosen a module tilt angle such that it largely compensates the Lorentz angle inclination of the charge drift. This maximizes the seed pixel charge, an important aspect after irradiation induced charge loss, but not optimal for position resolution. CMS instead has tuned for optimal charge sharing of its 100 × 150 μm2 pixels in the 100 μm direction. This leads to an excellent resolution of $\sigma_z = (12.7 \pm 2.3) \mu$m [5] for 100 μm pixel pitch (with a binary resolution of roughly 30 μm) as shown in Fig. 1(b) (top), almost as good as ATLAS ($\sigma_z \lesssim 10 \mu$m, $\sigma_z \approx 115 \mu$m) obtained with 50 μm pitch. The charge sharing is less effective in the orthogonal z-coordinate (150 μm pitch) where $\sigma_z = (28.1 \pm 1.9) \mu$m are obtained compared to 45 μm binary resolution. Increasing irradiation will, as a consequence, deteriorate the resolution more strongly for CMS [8].

The data taken so far with the three large LHC pixel detectors clearly justify the huge R&D effort that went into their development. The clean measurements of the beam spot position and its tilt, a complete mapping of materials by conversion finding and clean measurements of particle resonances like the J/ψ, important for the detector calibration, have been shown at this conference [9,10].

The LHC pixel Collaborations have started to plan for upgrades. While CMS plans for a completely new pixel detector with four barrel layers and 2 × 3 disks [11], ATLAS will add an innermost layer to be inserted into the existing three-layer detector exploiting the usage of a smaller beam pipe of 3 cm radius [12]. Later (~2020) completely new tracking detectors are planned by both experiments. A major goal is to half the material, i.e. 1.5% $X_0$/average per layer. To achieve this, apart from using light weight new material support structures, large efforts go into thinning of bumped chips [13] and new routing schemes exploiting 3D technology and through silicon vias (TSV) [13–15] which allow routing of R/O lines also on the backside of chips. Fig. 2(b) shows a successful thin chip assembly and a tapered TSV structure which is easier to realize on thin chips [13,14]. To address the expected increased rate by a factor of more than 3 and up to 10 compared to the design luminosity, a new front-end chip (FE-I4) has been designed [16] that can cope with the increased rate and needed bandwidth with excellent efficiency. For the sensors three options (planar Si, 3D silicon, CVD diamond) are studied which all have their advantages and disadvantages. Planar silicon sensors (n in n as well as n in p) [17] are best understood and are much lower in cost compared to other options. They require, however, voltages in excess of ~1000 V for full depletion after irradiation to

Table 1

<table>
<thead>
<tr>
<th>Luminosity (cm−2 s−1)</th>
<th>BX time (ns)</th>
<th>Part. rate (kHz/mm2)</th>
<th>Fluence (neq cm−2)</th>
<th>Ion. dose (kGy)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LHC</td>
<td>10−14</td>
<td>25</td>
<td>1000</td>
<td>10−15</td>
</tr>
<tr>
<td>SuperLHC</td>
<td>10−15</td>
<td>25 or 50</td>
<td>10 000</td>
<td>10−16</td>
</tr>
<tr>
<td>SuperKEKB</td>
<td>10−16</td>
<td>2</td>
<td>400</td>
<td>~3 × 10−12</td>
</tr>
<tr>
<td>ILC</td>
<td>10−14</td>
<td>350</td>
<td>250</td>
<td>10−12</td>
</tr>
<tr>
<td>RHIC</td>
<td>8 × 10−17</td>
<td>110</td>
<td>3.8</td>
<td>5 × 10−11</td>
</tr>
</tbody>
</table>

Fig. 1. (a) Measurement of the specific energy loss (dE/dx) with the ATLAS pixel detector [7]. (b) CMS space point resolution in the 100 μm pitch direction (top) and in the 150 μm pitch direction (bottom) as a function of the number of overlapping detector sites along the trajectory of a track [5].
3. New pixel trackers for new colliders

At rates somewhat lower and fluences as well as radiation doses much lower than at LHC and sLHC, active CMOS pixels and DEPFET pixels are very suitable devices for vertex detectors and are in fact planned at the heavy ion accelerator RHIC for the STAR experiment [21,22], at superKEKB for Belle II [23] and at SuperB [24]. Current generation CMOS pixel detectors like MAPS [25,26] allow electronics circuitry (mostly nMOS) within the active sensor area on the expense of diffusion based (small) signal charge collection, DEPFET pixels [27] have an amplification transistor implanted in a fully depleted bulk. Both of these approaches differ much from the above-mentioned hybrid pixel technology employed at the LHC. In particular, their readout is frame based with sequential row selection and parallel column readout provided by readout chip electronics located at the sensor edges rather than flipped atop the sensors. This results in the following common advantages: large area bump bonding and IC material in the active area is avoided, the active area of the sensor can be made very thin (~50 μm) resulting in a total material budget in the order of 0.2% X0. The consumed power is low due to the fact that only one or two rows is active at a time and hence less cooling is needed. Very small pixel linear dimensions (C<sub>N</sub> < 2 μm) are possible. For Belle II (DEPFET) the pixel size is limited by the data bandwidth which enormously increases by using very small and hence many pixels for the same area; therefore larger pixels (C<sub>N</sub> < 50 μm) are chosen. On the down side, MAPS and DEPFET technologies suffer from the larger vulnerability to radiation and lower readout speed compared to the hybrid pixel technology (see Table 1). Fig. 3 shows, as an example of these non-hybrid detectors, the DEPFET module concept for Belle II which employs backside etching for thickness reduction with the mechanical strength being supplied by the remaining frame [23]. Also shown at this conference was a new approach for efficient cooling in a SuperB pixel vertex detector using micro-channels [28], noting that the heat transfer coefficient is inversely proportional to the hydraulic diameter of a cooling channel.

![Fig. 2. (a) Charge collection efficiency (CCE) of n in p planar silicon pixel sensors (75 μm thick) as a function of bias voltage after irradiation for 1 (black), 3 (red) and 10 (green) × 10<sup>16</sup> n<sub>n</sub><sub>e</sub>/cm<sup>2</sup> [15]. (b) SEM photograph of a bumped chip-sensor assembly with a thinned (90 μm) large area FE chip and sketch of a tapered TSV with SEM photo [13]. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)](image)

![Fig. 3. (a) DEPFET module with thinned sensor in support frame. (b) Photograph of a DEPFET prototype module with steering and R/O chips on PCB board [23].](image)
Finally, planning and R&D for a future Linear Collider target material thicknesses and spatial resolutions even beyond what was discussed here so far, in order to achieve impact parameter resolutions of below $\sim 10 \, \mu m$ even at low ($\sim 2 \, GeV$) momenta. The dedicated PLUME Collaboration investigates ultra low weight support structures in this context.

4. Imaging with pixel detectors at synchrotron light sources

Huge progress was reported at this conference regarding pixel detector imaging in synchrotron light experiments. One application is sketched in Fig. 4(a) – a typical diffraction experiment. The development of hybrid pixel detectors has also largely enriched the possibilities in synchrotron light imaging. To stay with the example, the detection of diffraction patterns requires complete area imaging of spots of different intensities with high picture rates. For counting pixel detectors, this in turn means: $> MHz$ rates per pixel, frame rates above kHz at a light source, 5 MHz at an XFEL, with no or little dead time, very large dynamic range (up to $10^6$), small pixel size ($< 50 \, \mu m$), and seamless detectors with no dead areas. The PILATUS detector has pioneered the use of pixel detectors for synchrotron light imaging with great success as reported at this conference [33]. With this device, which is now also commercially available, the dynamic range for photon detection has been increased from 15–16 bit (CCD detectors) to 20 bit. Continuous shutter-free data collection with the possibility of angle-slicing and simultaneous high and low exposure data taking at room temperature have been made possible with PILATUS. At count rates of several MHz per pixel, the frame rates are still fairly low ($12.5 \, Hz$) with 3 ms dead time. The next generation of a hybrid pixel synchrotron light imager is EIGER [34]. The functioning readout chip prototype has been presented [34], featuring smaller pixels ($75 \times 75 \, \mu m^2$) and thus larger count rate per mm$^2$, much larger frame rates ($> 20 \, kHz$), and continuous, quasi dead time free readout. A key feature is the buffering of a complete frame (see Fig. 5) while continued readout takes place. Fig. 5 also shows an X-ray image of a flower taken with EIGER. Energy-selective synchrotron light imaging has been reported from Spring-8 experiments in Japan using a threshold scanning method of PILATUS [35] or by a new pixel device using CdTe as sensor material and a readout chip with a window comparator selecting an energy window [36].

What is different regarding photon detection when doing experiments at an X-ray free electron laser (XFEL)? This is illustrated in Fig. 4(b). While in conventional synchrotron light sources the X-ray photons arrive in a large number of photon bunches with low intensity irregularly distributed in time, in an XFEL they arrive coherently in trains of extremely short 100 fs bunches separated in time by 200 ns. This leads to the challenging requirement to cope with a huge dynamic range for detecting photons from a few up to 10 000 per 200 ns, which translates into frame rates of 5 MHz. Imaging at XFELs thus requires either new counting methods or more advanced integrating detector readout concepts. Current approaches use a switching characteristic for counting devices (GOTTHARD, AGIPD) [31] or a very non-linear device characteristic leading to signal compression in the integrating DSSC device [37]. Fig. 6 illustrates both concepts. For the counting readout of GOTTHARD (strips) or AGIPD (pixels) the amplifier gain is switched in a threshold driven way leading to different slopes of the characteristics when the photon flux is high (solid lines in Fig. 6(b)) or low (dashed lines). For the integrating

---

**Fig. 4.** (a) Diffraction is a typical example of experiments at synchrotron light sources (illustration). (b) Sketch of the different beam situations at a synchrotron light source compared to an X-ray free electron laser situation [31].

**Fig. 5.** (top) Double buffering cell within the EIGER-chip [34] allows continuous, quasi dead time free readout in synchrotron light imaging with hybrid pixel detectors. (bottom) Real and X-ray image of a flower obtained with EIGER [34].
Detector development in photon science at the various X-ray sources (FLASH, SCSS, LCLS, FERMI, XFEL) is being addressed within the newly formed CFEL organization [39] in Hamburg, Germany and first imaging experiments at LCLS using modified pnCCDs of MPI-Munich [40] were reported [39].

5. News towards fully monolithic pixel devices

A fully monolithic pixel device, featuring full charge collection by drift in a depleted bulk, full CMOS electronics in the active area and perhaps even 3D integration allowing the stacking of additional electronic layers, has been the goal of intense R&D in the past decade with remarkable successes. The Monolithic Active Pixel Sensors (MAPS) concept [26] has paved the way so far, but this technology also suffers from small and incomplete signal charge collected by diffusion rather than drift and by the fact that the charge collecting n-well must compete with other n-wells if pMOST transistors are included in the active area, i.e. full CMOS electronics has not yet been achieved over the entire active area. To address this the deep n-well [41,24] process pursued by the Pisa group creates a large n-well which acts as the charge collecting diode and has an imbedded p-well housing the nMOS transistors while the pMOS transistors are in a n-well which is geometrically smaller and less deep than the charge collecting deep n-well. Further progress on this approach using the small 65 nm technology has been reported at this conference [42]. The 180 nm INMAPS quadruple well process used by the Rutherford group [43] employs a deep p-well placed underneath the pMOSTs containing n-well thus shielding it from acting as a charge drain. While these improvements yield already larger $S/N$ ratios than with standard MAPS, the diffusion based charge collection and the only moderate radiation resistance have provoked further studies. Reported here [22,43] were attempts with a larger charge collecting diode and a new process feature providing a higher resistivity ($\sim 1 \text{k}\Omega \text{cm}$) epitaxial layer for faster and more efficient charge collection. Charge collection efficiencies close to 100%, $S/N$ values of $\sim 30$ [22] and $\sim 90$ [43], respectively, have been obtained. In addition, the radiation tolerance was improved by a factor of about 100 [43].

In a completely new approach [44], fairly complete characterization results have been reported [45] at this conference which are quite striking. Fig. 8(a) shows the principle. The AMS 0.35 $\mu$m HV technology employing high-voltage n-wells in a p-substrate is used to create a monolithic pixel sensor which features full charge collection by drift in a directional E-field, 100% fill factor without charge loss due to embedding the entire structure (nMOST and pMOST in n-wells) in a deep n-well. Further progress on this approach using the small 65 nm technology has been reported at this conference [42]. The 180 nm INMAPS quadruple well process used by the Rutherford group [43] employs a deep p-well placed underneath the pMOSTs containing n-well thus shielding it from acting as a charge drain. While these improvements yield already larger $S/N$ ratios than with standard MAPS, the diffusion based charge collection and the only moderate radiation resistance have provoked further studies. Reported here [22,43] were attempts with a larger charge collecting diode and a new process feature providing a higher resistivity ($\sim 1 \text{k}\Omega \text{cm}$) epitaxial layer for faster and more efficient charge collection. Charge collection efficiencies close to 100%, $S/N$ values of $\sim 30$ [22] and $\sim 90$ [43], respectively, have been obtained. In addition, the radiation tolerance was improved by a factor of about 100 [43].

In a completely new approach [44], fairly complete characterization results have been reported [45] at this conference which are quite striking. Fig. 8(a) shows the principle. The AMS 0.35 $\mu$m HV technology employing high-voltage n-wells in a p-substrate is used to create a monolithic pixel sensor which features full charge collection by drift in a directional E-field, 100% fill factor without charge loss due to embedding the entire structure (nMOST and pMOST in n-wells) in a deep n-well which also is the collecting diode. The device is radiation hard up to fluxes of $10^{15} \text{Heq cm}^{-2}$ as shown in Fig. 8(b) which shows the response to a 53Fe source (6 keV X-ray) before and after high fluence irradiation ($T = 10^3 \text{C}$). The signal is widened but the irradiated spectrum (Fig. 8(b)) shows a comfortable distance between the narrow pedestal peak and the signal of 1660e$^-$. This way many of the goals mentioned above for a monolithic detector are met: fast and $\sim$ full charge collection, true CMOS circuitry inside the active area, large $S/N$ ratio ($\sim 100$), small pixel size ($21 \times 21 \mu\text{m}^2$), and high radiation hardness (to $10^{15} \text{Heq cm}^{-2}$), at a power of about 12 $\mu$W per pixel [45].

The other important and promising approach to monolithic pixel devices is the Silicon-on-Insulator technology (SOI) progress

DSSC device, the DEPFET pixel concept mentioned earlier is employed [37]: The internal electron collecting gate steers the channel current of the implanted transistor with the gain depending on the (capacitive) coupling of the internal gate to the channel. Hence, in a geometrically large and appropriately shaped internal gate, obtained by a decreasing n-doping profile (see Fig. 6(c) (left)), the current gain depends non-linearly on the filling level leading to the characteristic sketched in Fig. 6(c), right. Another interesting R&D towards the required large photon dynamic range at XFELs was presented [38] which exploits the possibilities of the SOI technology. As sketched in Fig. 7 both different combinations of the charge collecting nodes and different gain stages (low, middle, high) are used.
which was also reported at this conference [46–48,38]. The SOI technology promises full CMOS circuitry in the active area without bump bonding with high sensitivity and full charge collection. Using an industrial process offers reliability and the smooth connection to the 3D integration technology which is currently of common interest in many groups. Fig. 9(a) shows an example SOI structure consisting of a high resistivity substrate, wafer bonded to a CMOS layer separated by a buried oxide layer (BOX), through which vias connect to the substrate. The main technical issues of the SOI technology are or have been (a) a reliable fabrication process, (b) the question of how to avoid the backgate effect (see below), (c) radiation hardness due to hole trapping inside the BOX, and (d) the attainable resistivity of the substrate material. These are currently being addressed, especially at OKI [47]. As was shown at this conference, hole trapping in the box can to some extent be compensated by changing the substrate voltage [48]. Several R&D efforts have been reported [47] done at OKI in collaboration with Fermilab to address in particular the backgate effect (by an additional buried p-well structure), cross talk (by implementing nested wells, i.e. deep buried p-well, buried n-well, or by a double SOI structure), and the radiation hardness (by double SOI layer wafers providing a biasable intermediate conducting layer that compensates built-up oxid charges), all sketched in Fig. 9(b) and (c). It is shown that indeed the backgate effect is suppressed by buried p-well structures. The next generation of tested devices and their performance in particle beams could be very interesting. Finally, the experience of the past years with 3D integration efforts led by Fermilab was reported [49]. The various efforts with Tezzaron/Chartered, MIT-Lincoln Lab and OKI have shown that a long term commitment is needed with slow, step-wise successes. On the long run, however, a combination of monolithic devices (SOI or CMOS active pixels) combined with 3D integration will probably be the path to go.

6. Conclusions

Pixel 2010 was the fifth very successful international conference in this series. It has bought out the excellent performance
demonstration of the LHC pixel detectors, the progresses made in imaging applications, especially those at synchrotron light sources and XFELs, and has shown new interesting R&D ideas and realizations that will advance the pixel technology further in the coming years. We are looking forward to the next conference, most likely in Japan.

Acknowledgments

The author would like to thank the organizers of this wonderful conference with its excellent location and its spectacular realizations that will advance the pixel technology further in the coming years. We are looking forward to the next conference, most likely in Japan.

References

[38] T. Hatsui, Development of multi-via pixel with signal charge division to realize high effective 105 dynamic range for X-ray free-electron laser applications, Nucl. Instr. and Meth. A, submitted for publication.